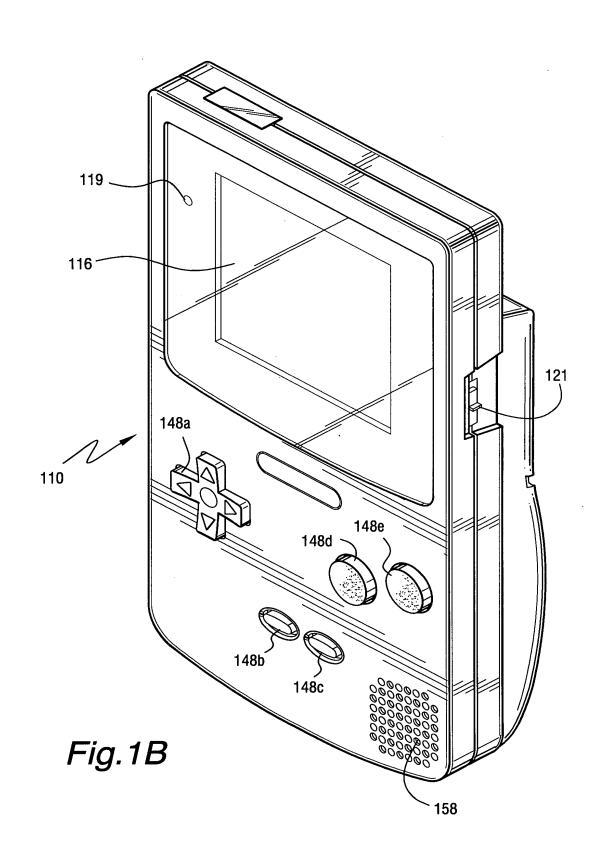


Fig.1A



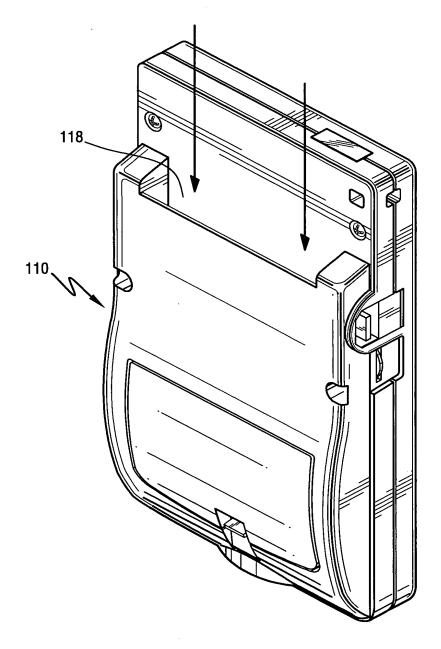
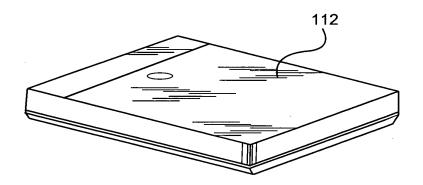
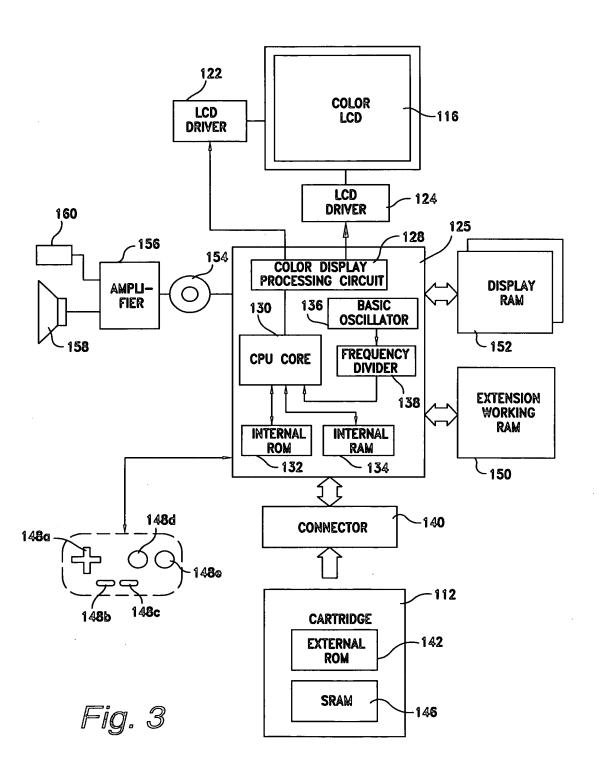
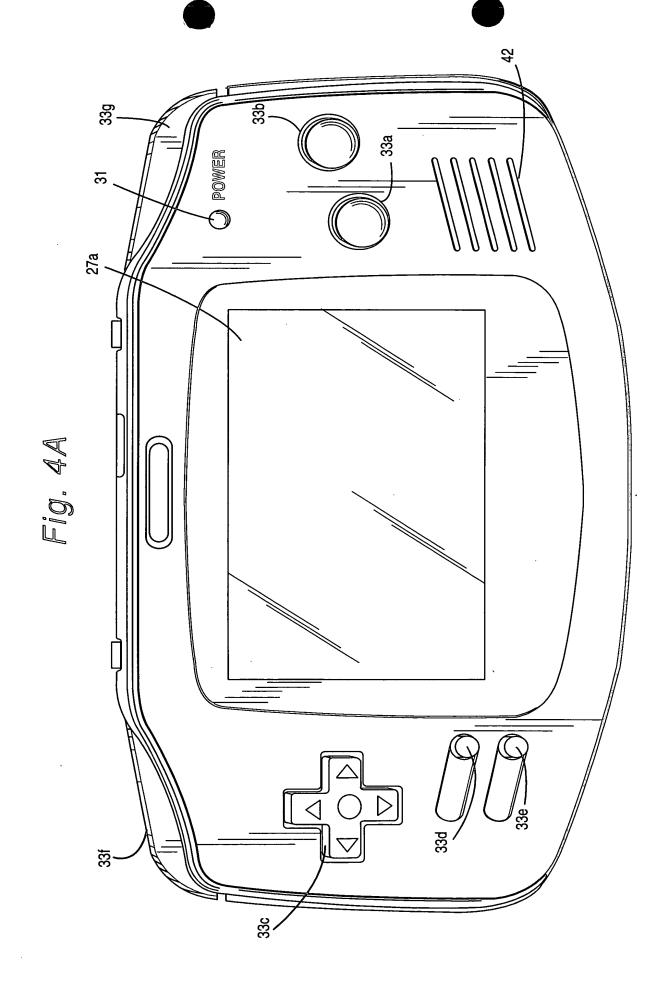


Fig.1C

Fig. 2
(Prior Art)







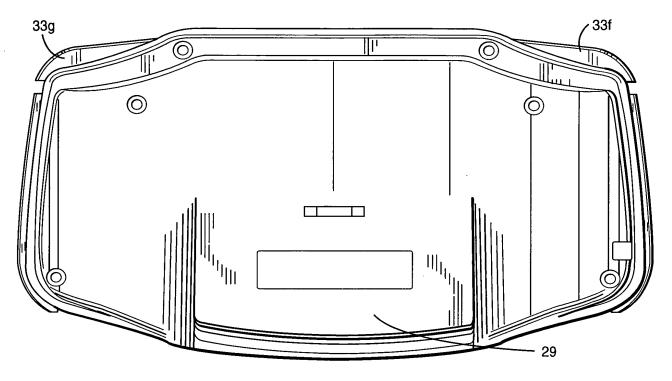


Fig. 4B

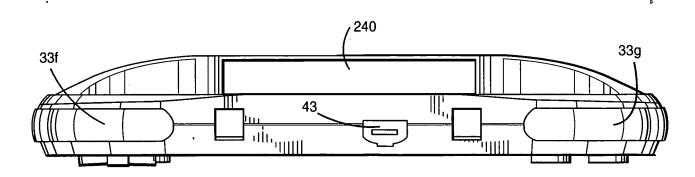


Fig. 4C

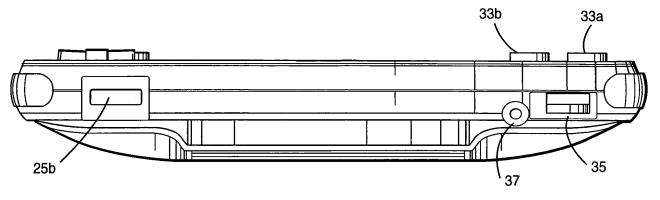
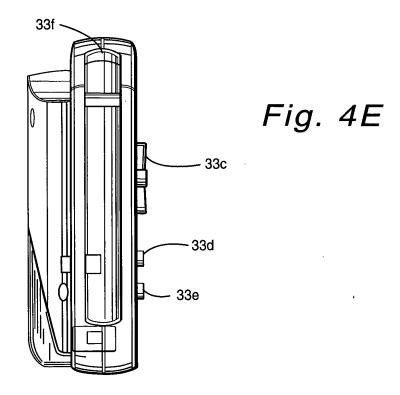


Fig. 4D



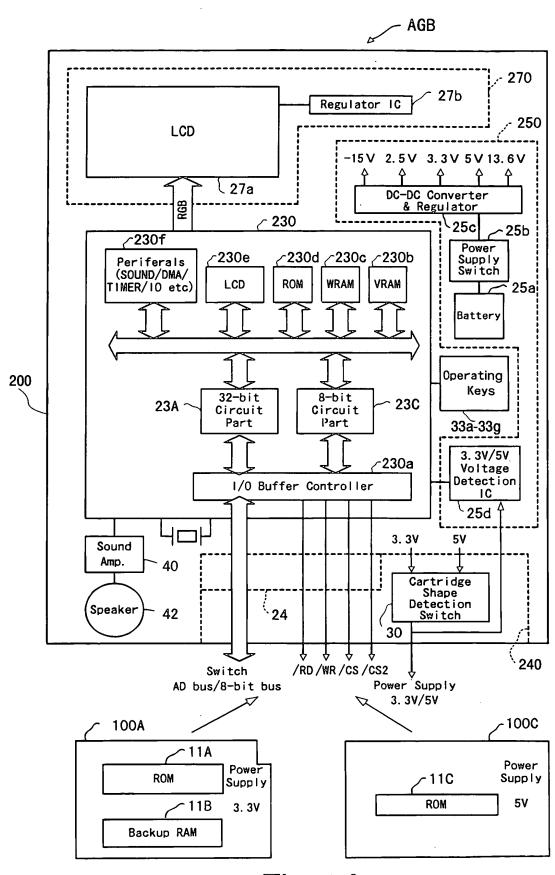
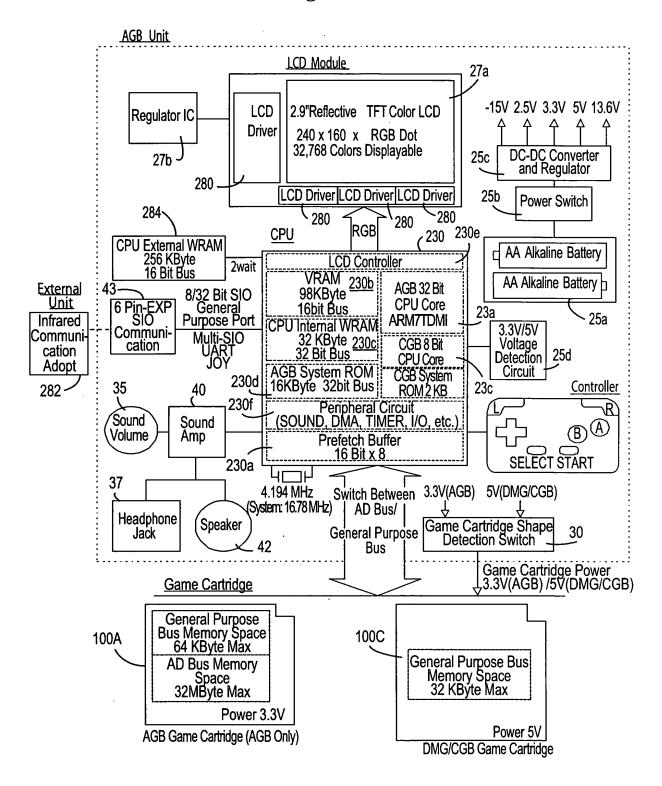
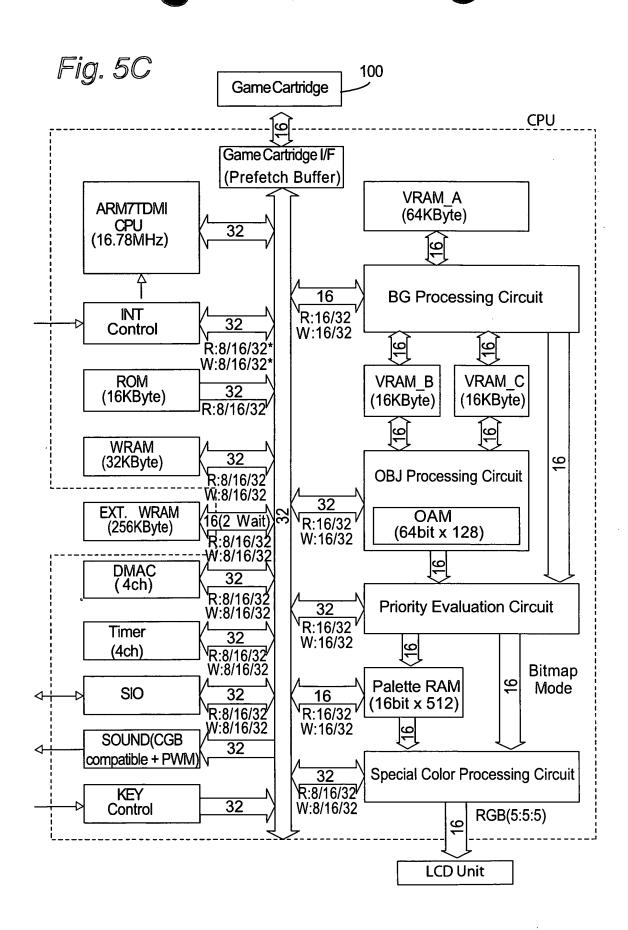


Fig. 5A

Fig. 5B





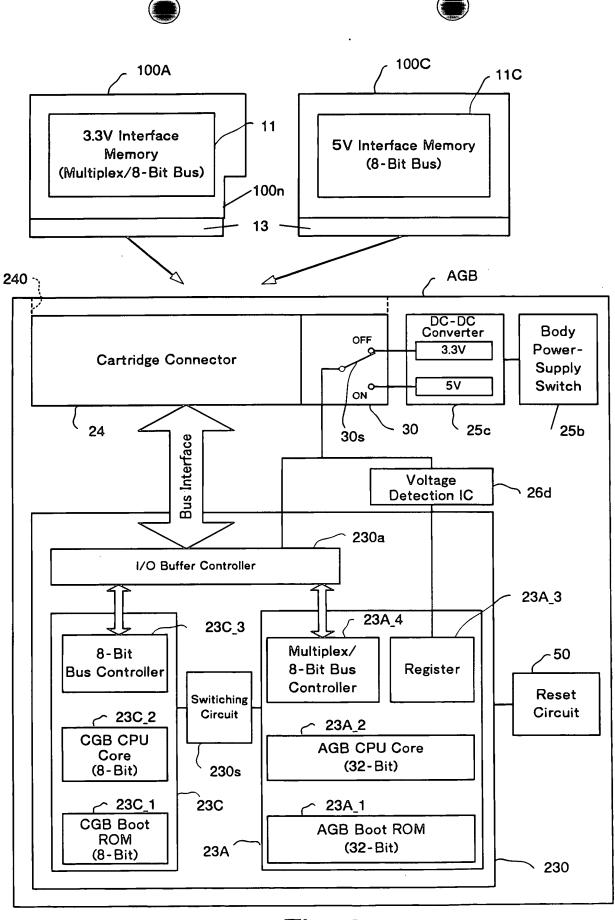
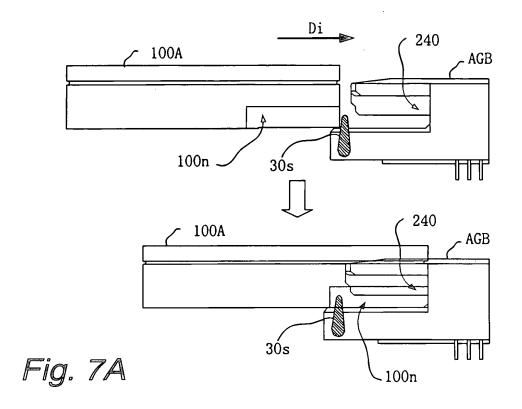
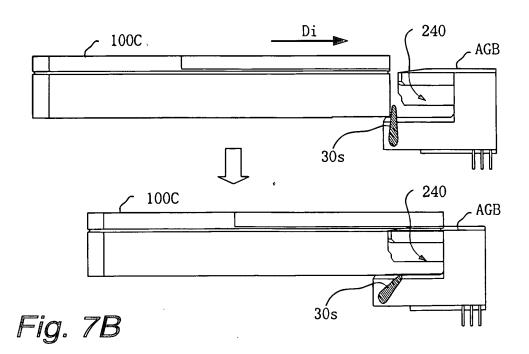
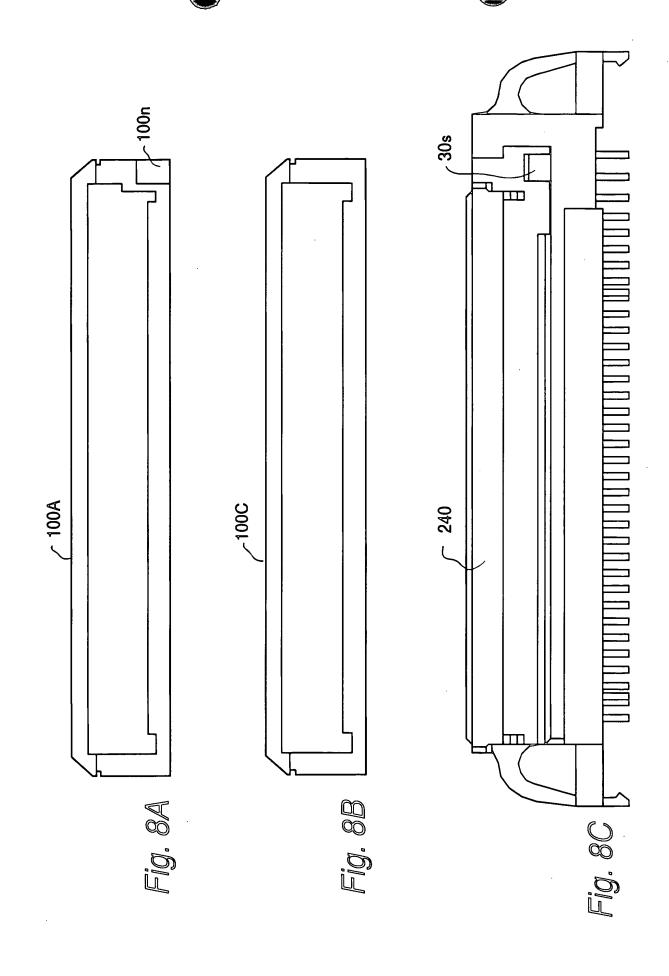
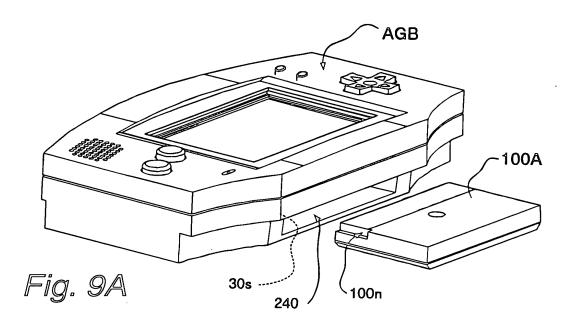


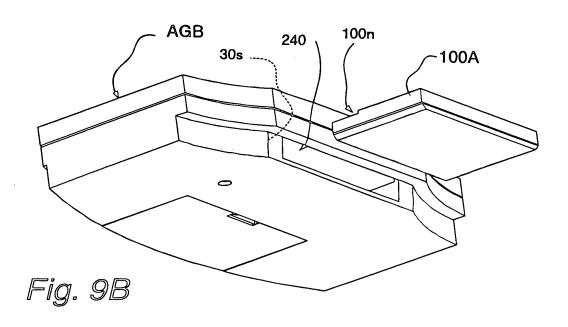
Fig. 6

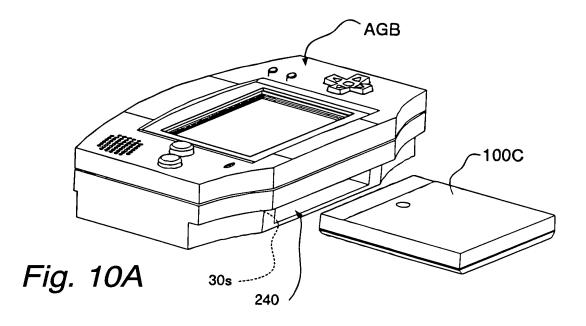


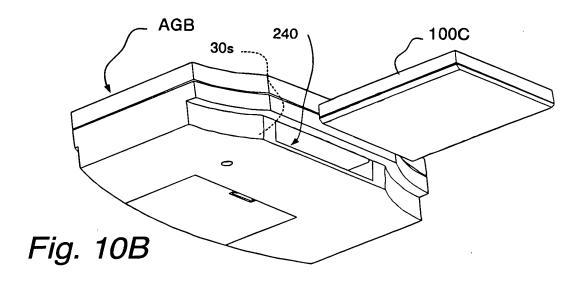


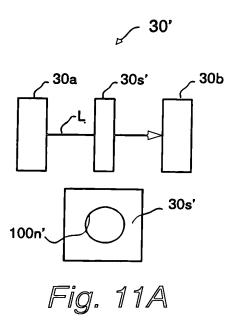


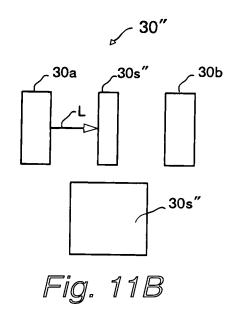


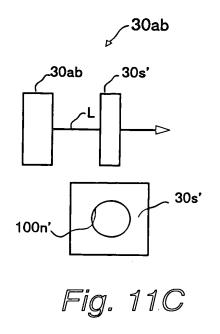


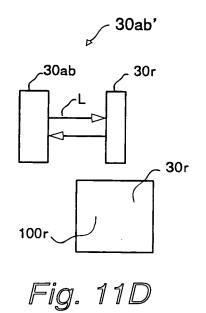












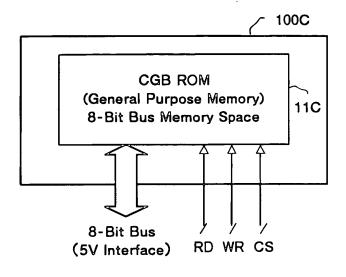


Fig. 12A

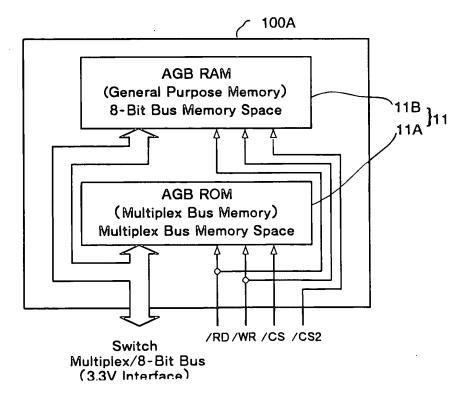
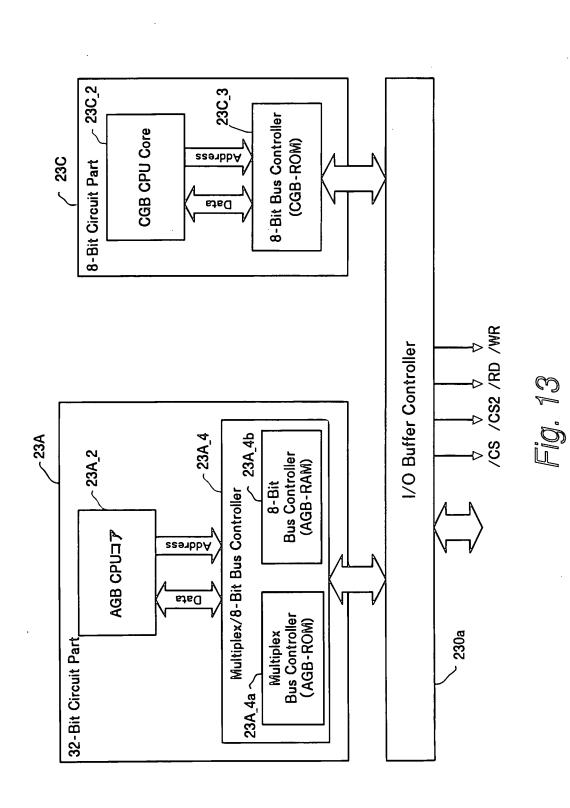


Fig. 12B



()

Fig. 14

NO	CGB	ACR BORA	AGB RAM	Domeste	
				Remarks	
1	VDD(5V)	VDD(3.3V)	VDD(3.3V)	Switch Voltage By Detection Switch	
2	PHI	PHI	PHI		
3	/WR	/WR	/WR		
4	/RD	/RD	/RD		
5	/CS	/CS	/CS	Select ROM Chip	
6	A0	A0/DO	A0	Address/Data Shared Terminal	
7	A1	A1/D1	A1	Same As Above	
8	A2	A2/D2	A2	Same As Above	
9	A3	A3/D3	A3	Same As Above	
10	A4	A4/D4	A4	Same As Above	
11	A5	A5/D5	A5	Same As Above	
12	A6	A6/D6	A6	Same As Above	
13	A7	A7/D7	A7	Same As Above	
14	A8	A8/D8	A8	Same As Above	
15	A9	A9/D9	A9	Same As Above	
16	A10	A10/D10	A10	Same As Above	
17	A11	A11/D11	A11	Same As Above	
18	A12	A12/D12	A12	Same As Above	
19	A13	A13/D13	A13	Same As Above	
20	A14	A14/D14	A14	Same As Above	
21	A15	A15/D15	A15	Same As Above	
22	D0	A16	D0		
23	D1	A17	D1		
24	D2	A18	D2		
25	D3	A19	D3		
26	D4	A20	D4		
27	D5	A21	D5		
28	D6	A22	D6		
29	D7	A23	D7		
30	/RES	/CS2	/CS2	Action Each Different In AGB and CGB Modes	
31	Not Allowed to Use (VIN)	IREQ/ DREQ	IREQ/ DREQ	In CGB Mode, Ignore VIN Input	
32	GND	GND	GND		

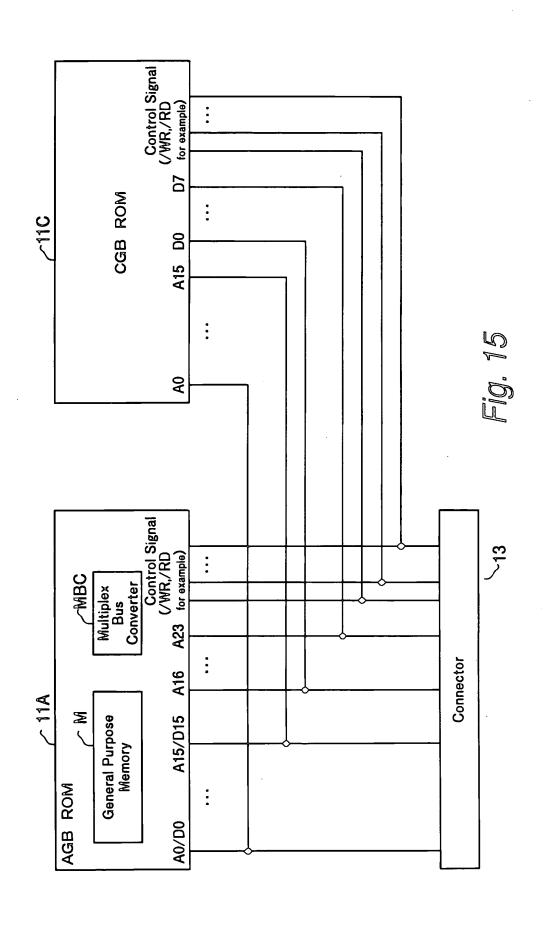


Fig. 16A

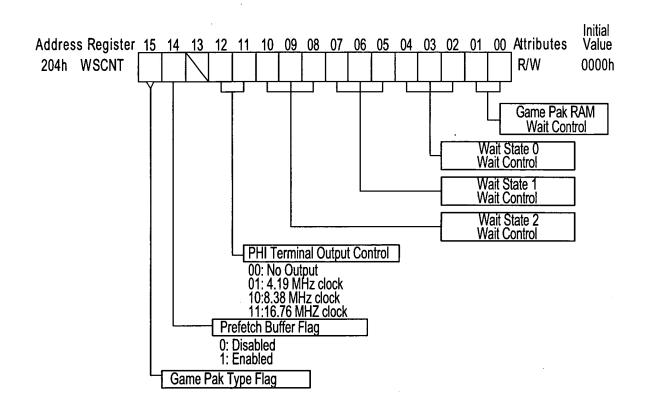
Fig. 16C

0E00FFFFh		FFFFh	
0E000000h	AGB RAM 11B		
CLOGOGOGII	AGB ROM 11A	·	CGB ROM 11C
08000000h		8000h	
	Internal ROM		Internal ROM
	Internal RAM I/O Register, and the like		Internal RAM I/O Register, and the like
00000000h		0000h	

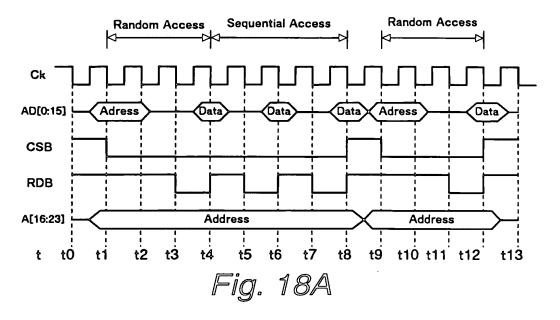
Fig. 16B

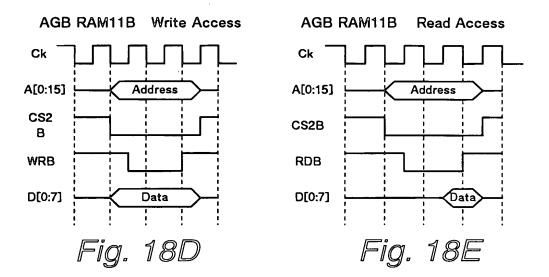
	0FFFFFFh		
	0E00FFFFh	Game Pak RAM	
•	0E000000h	(0-512 Kbits)	Images
	0DFFFFFFh	Game Pak ROM	Flash Memory (1 Mbit)
		Wait State 2	/// Mask ROM///
	0C000000h	(32 MB)	////(255Mbits)///
	OBFFFFFh	0 01004	Flash Memory
	ODITITIO	Game Pak ROM Wait State 1	(TIVIDIL)
		(32 MB)	/// Mask ROM///
	0A000000h	(32 1410)	////(255Mbits)///
	09FFFFFFh	Game Pak ROM	Flash Memory
		Wait State 0	(1 Mbit)
Cama Dak Mamani		(32 MB)	Mask ROM//(255 Mbits)///
Game_Pak_Memory_ AGB Internal	_08000000b	· · · · · · · · · · · · · · · · · · ·	[//// ²⁵⁰ ////////////////////////////////////
Memory	070003FFh	OAM	
•	0700001111 070000000h	(1 Kbyte)	
	010000001		
	06017FFFh	\/DA14	
		VRAM (96 Kbytes)	
	06000000h	(30 KDyles)	
	000000001		
	050003FFh	Palette RAM (1 Kbyte)	
	<u>05000000h</u>	(1 Kbyte)	
	040000006	I/O, Registers	
	<u>04000000h</u>	11111111	
	03007FFFh	001114	
	0000711111	CPU Internal Working RAM	
	_03000000h	(32 Kbytes)	
	0203FFFFh	CDI Externel Marking DAM	
		CPU External Working RAM (256 Kbytes)	[777] ROM
	02000000h	(200 : 10) (00)	RAM
	00003FFFh	System ROM///	Unused Area
	<u>00000000h</u>	//// (16 Kbytes)////	Image Area
			<u> </u>

Fig. 17



AGB ROM11A Read Access





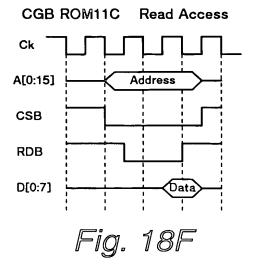


Fig. 18B

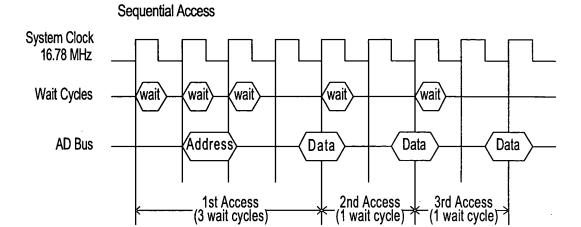
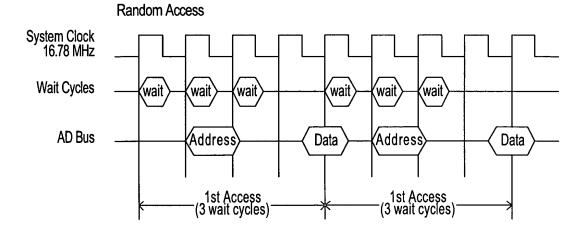


Fig. 18C



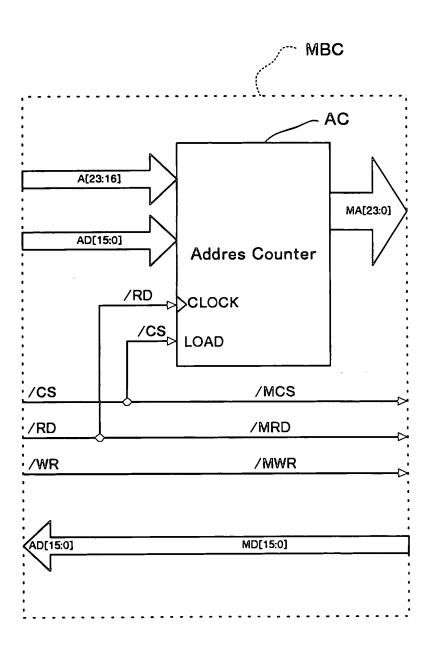
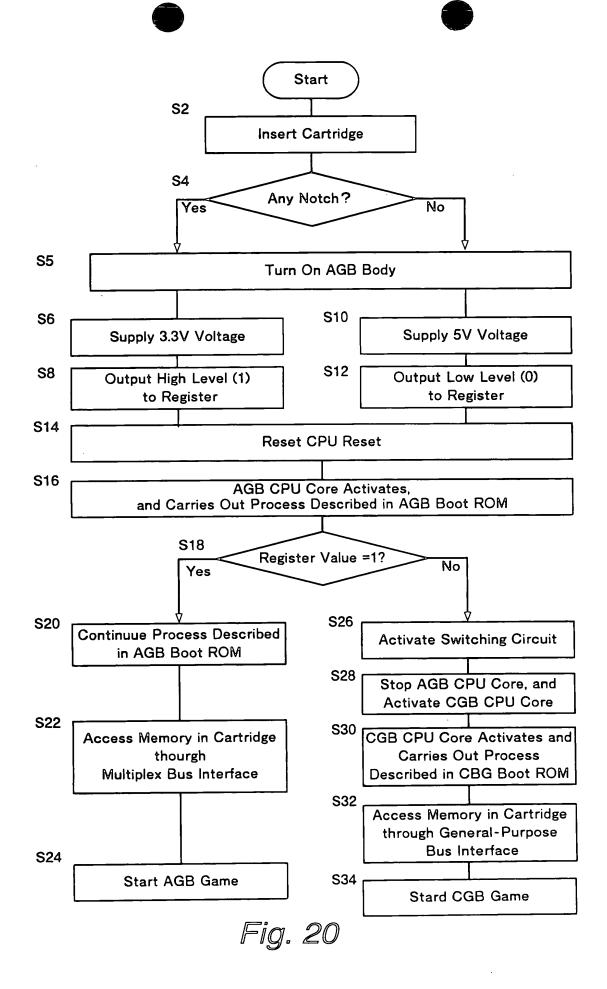


Fig. 19



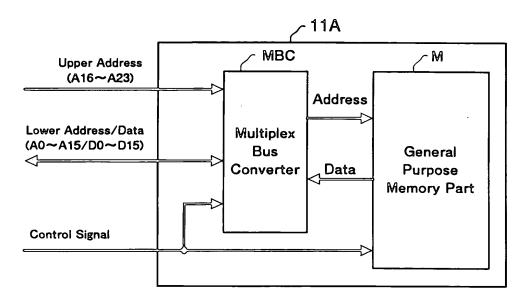


Fig. 21A

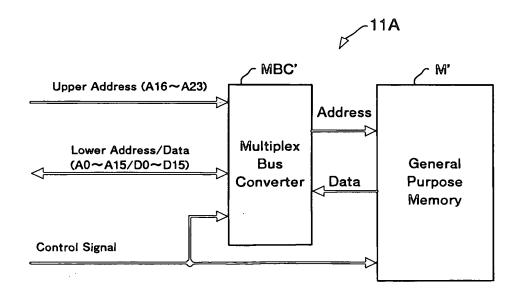


Fig. 21B

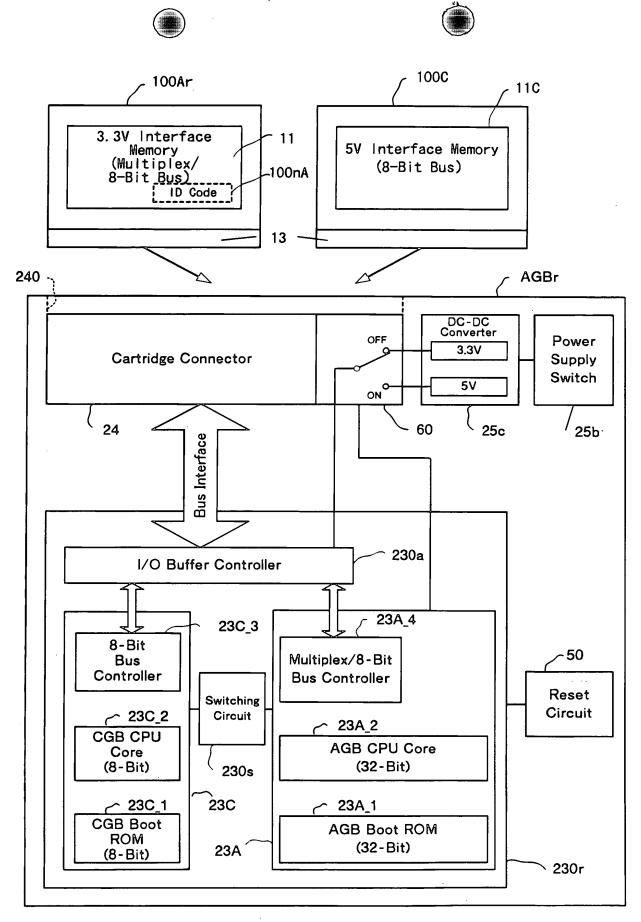
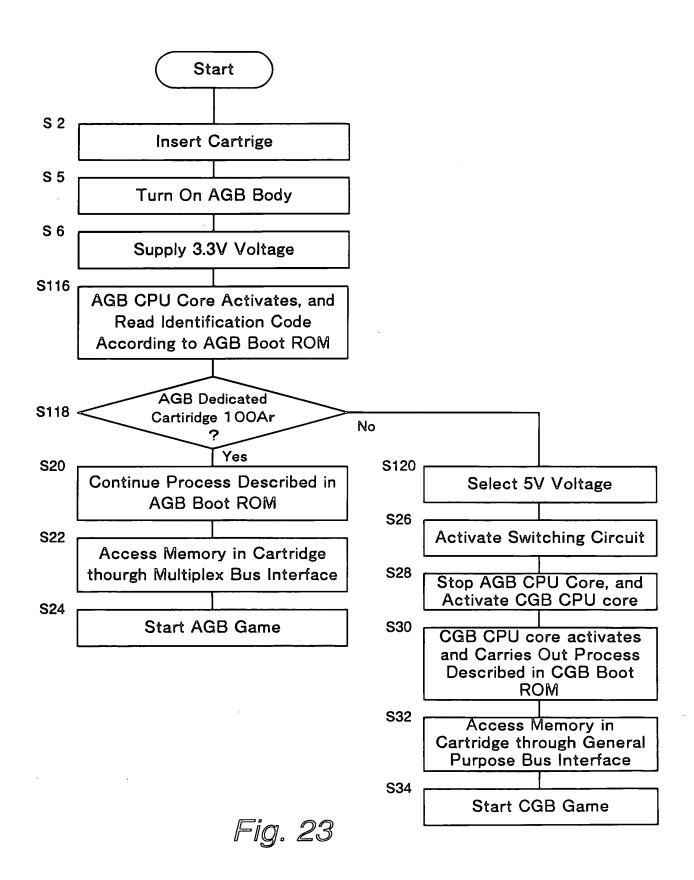


Fig. 22



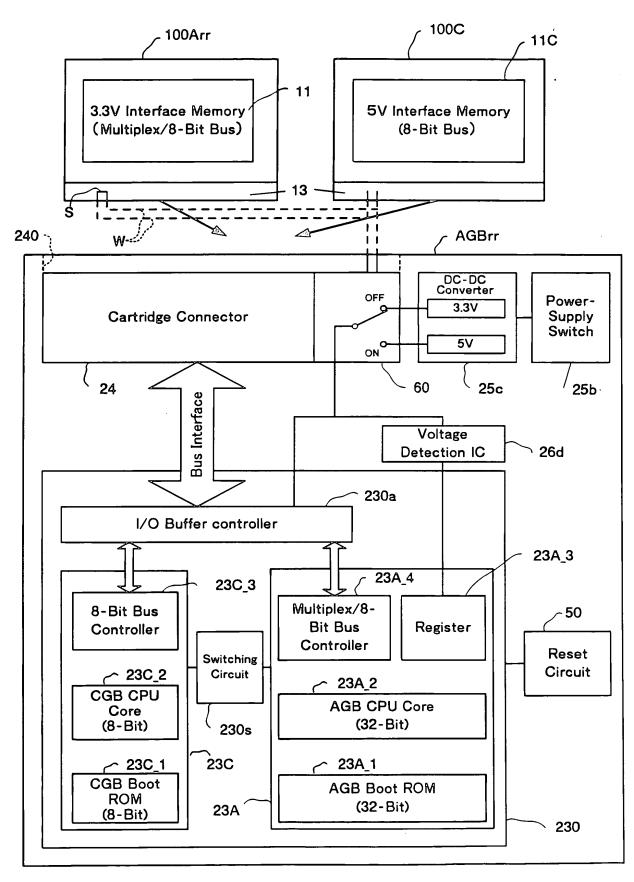


Fig. 24

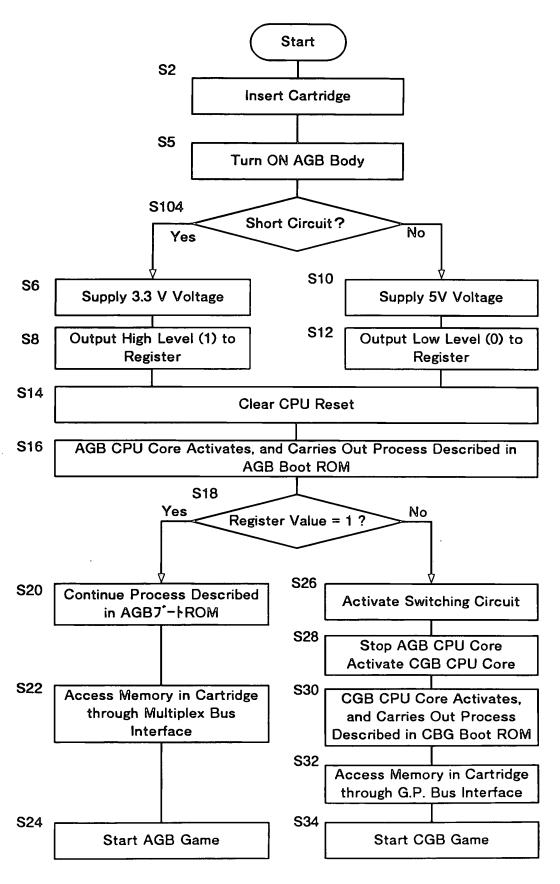
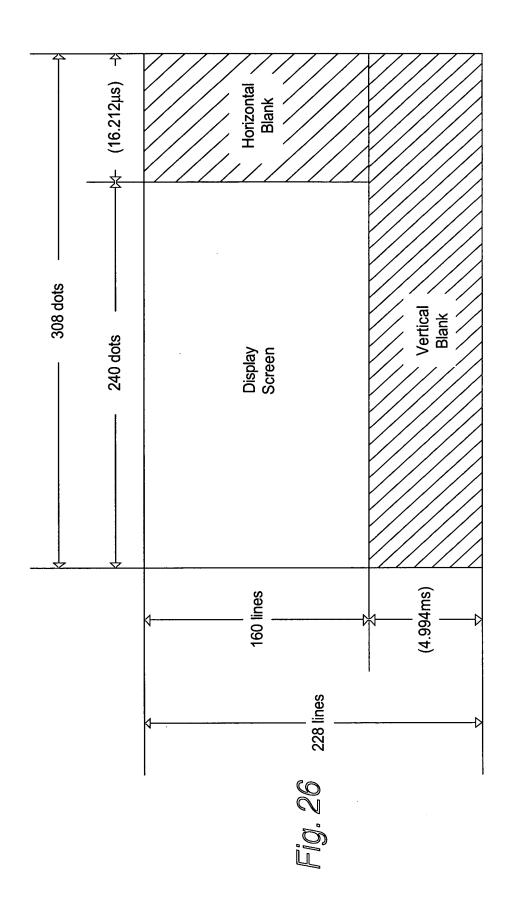
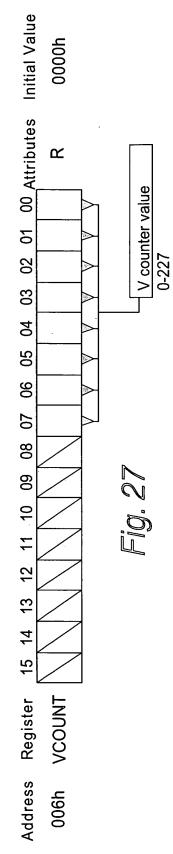


Fig. 25





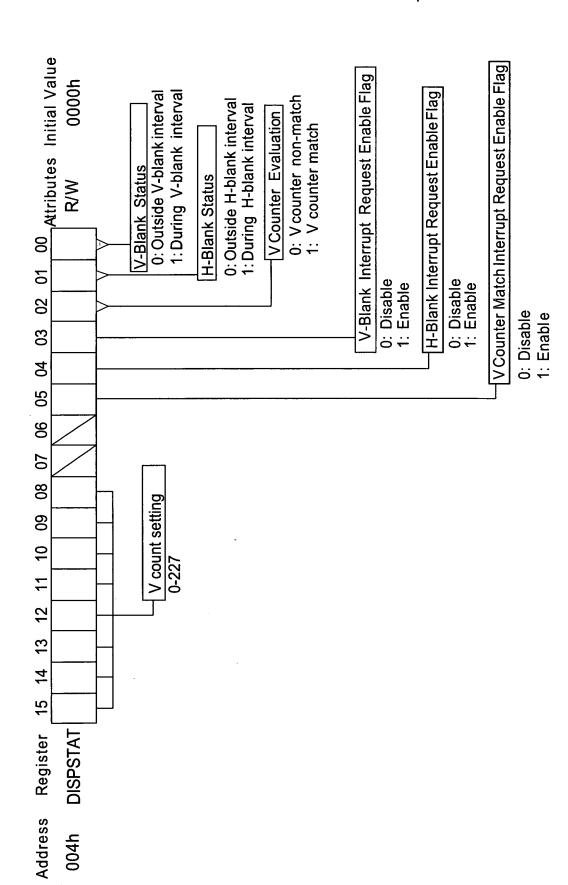


FIG. 28

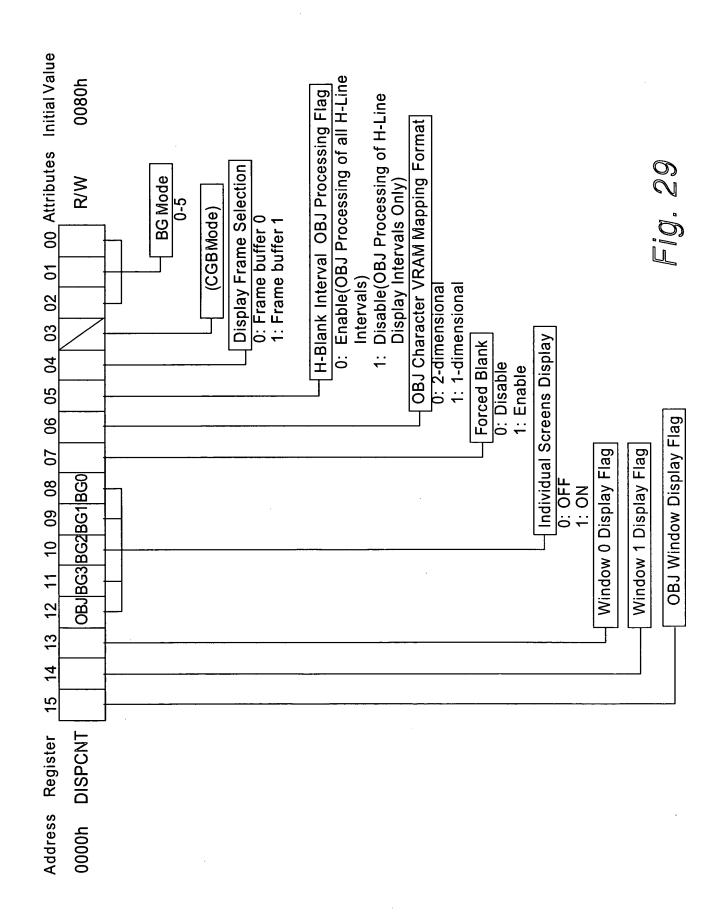


Fig. 30A

LC Mode	Characte	Character Format BG Screen	Screen	Number of	Number of Colors/		_	-eatı	Features		
DOM: DO	Rotation/ scaling	No. of Screens	Size	Specifiable	Palettes	*	*2	*3	*1 *2 *3 *4 *5 *6	*5	*6
C	ÖZ	7	526 x 256	1024	16/16	O	C	C		0	0
>		+	512 X 512	1027	256/1))	>	>	>)
	QN C	í	256 x 256	4024	16/16	C	C	(0	(
	2	7	512×512	1024	256/1)	>	>	>	>)
-	γον	1	128 x 128	256	256/1	0	>	0	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	0	C
	<u>S</u>	-	1024 × 1024	230	200/ 1	>	<	>	>	>)
۲	, ,	C	128 x 128	996	75614	C	>	-	>	(0
7	165	7	1024 × 1024	230	730/ 1)	\	>	0)	O

*1 HV Scroll (individual screens)
*2 HV Flip (individual characters)
*3 Mosaic (16 levels)

*4 Semi-transparent (16 levels)
*5 Fade-in/Fade-out
*6 Screen priority specification (2 bits)

Fig. 30B

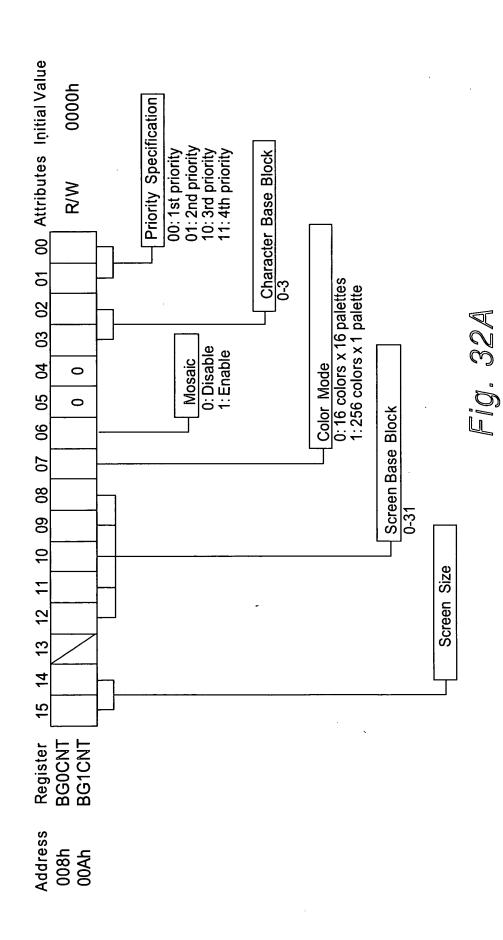
	Bitmap	Bitmap Format BG Screen	Screen	, and a second			ш	Features	Ires		
BG Mode	Rotation/ Scaling	No. of Screens	Size	Memory	No. of Colors	*	*2	*1 *2 *3 *4 *5 *6	*4	*5	9*
3	Yes	1	240 x 160	_	32,768	0	×	0 0 0 0 x 0	0	0	0
4	Yes	1	240×160	2	256	0	×	0 0 0 0 x 0	0	0	0
5	Yes	1	160 x 128	2	32,768	0 0 0 0 X 0	×	0	0	0	0

^{*1} HV Scroll (individual screens)
*2 HV Flip (individual characters)
*3 Mosaic (16 levels)

^{*4} Semi-transparent (16 levels)
*5 Fade-in/Fade-out
*6 Screen priority specification (2 bits)

	BG Modes 0, 1, and 2		BG Mode 3		BG Modes 4 and 5
06017FFFh	OBJ Character Data	06014000h	OBJ Character Data 16 Kbytes	06014000h	OBJ Character Data 16 Kbytes
06010000h	32 Kbytes				
					Frame Buffer 1 40 Kbytes
	BG0-BG3 Screen Data Maximum 32 Kbytes		Frame Buffer 0 80 Kbytes	0600A000h	
	and				
	BG0-BG3 Shared Character Data Minimum 32 Kbytes				Frame Buffer 0 40 Kbytes
000000090					

Fig. 31



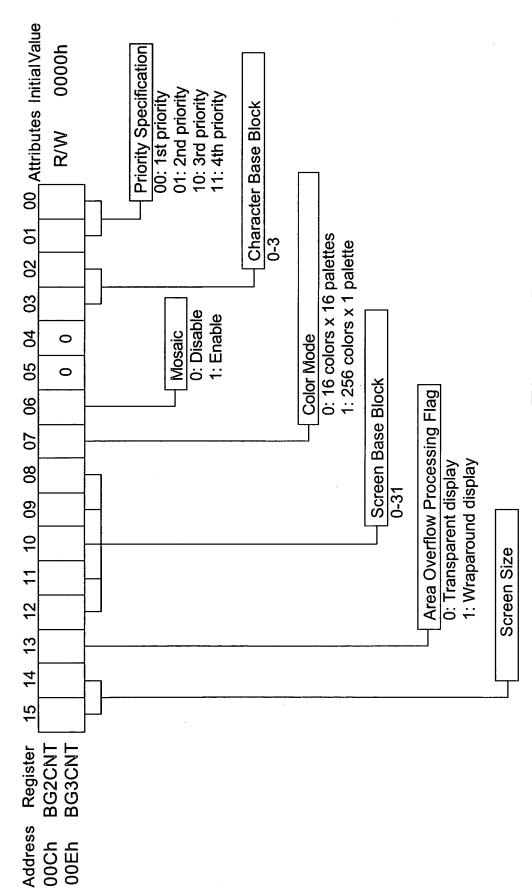
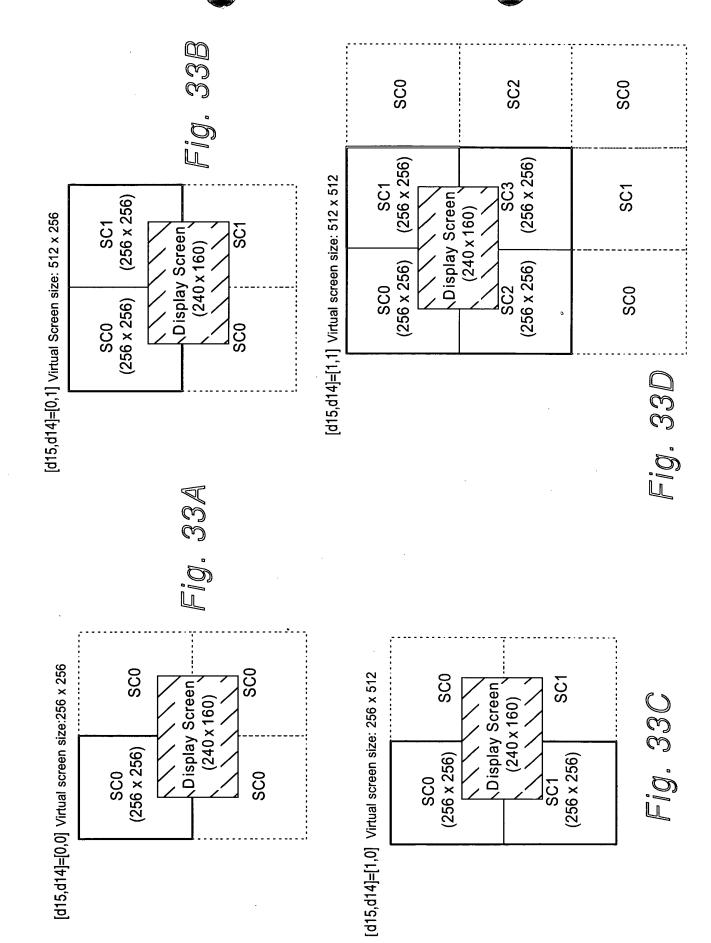


Fig. 32B



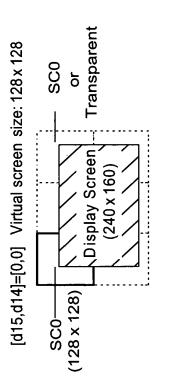


Fig. 34A

[d15,d14]=[0,1] Virtual screen size: 256 x 256

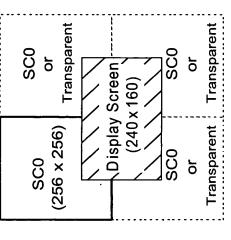


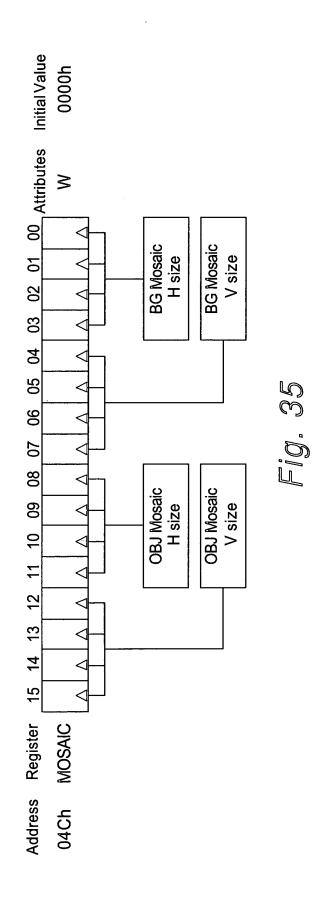
Fig. 34B

SCO
(512 x 512)
SCO
(512 x 512)
SCO
(240 x 160)
(240 x 160)
SCO
or
Transparent
Transparent
Transparent
Transparent

SCO (1024 x 1024)
SCO (1024 x 1024)
SCO or Transparent (240 x 160)
SCO or Transparent Transparent Transparent Transparent

Fig. 34D

Fig. 340



Normal Display

9

00 00 05

00 00

18 19 28 29 38 39

24

22

20

Mosaic H size: 3 V size: 5

08

04						64
00	00	00	00	00	00	
00	00	00	00	00	00	
00 00 00 00	00	00 00 00	00 00	00 00 00	00 00 00 00	
00	00	00	00	00	00	09
80		28		48		89
90		26		46		99

44

42

40

40 41

64

62

9

Fig. 36A

50 | 51 | 52 | 53 | 54 | 55 | 56 | 57 |

Fig. 36B

Fig. 36C

68

BG Character Data Base Block

BG Screen Data Base Block

	=	
OBJ Character Data 32 Kbytes	10000h	OBJ Character Data 32 Kbytes
	1000011	
		Base Block 31
		Base Block 30
		Base Block 29
Base Block 3		Base Block 28
Base Block o		Base Block 27
		Base Block 26
		Base Block 25
	C000h	Base Block 24
		Base Block 23
		Base Block 22
		Base Block 21
Base Block 2		Base Block 20
Base Block 2		Base Block 19
		Base Block 18
		Base Block 17
	. 8000h	Base Block 16
	T	Base Block 15
1		Base Block 14
		Base Block 13
Base Block 1		Base Block 12
Base Block I		Base Block 11
		Base Block 10
		Base Block 09
	4000h	Base Block 08
	T	Base Block 07
		Base Block 06
		Base Block 05
Base Block 0		Base Block 04
Dase block o		Base Block 03
		Base Block 02
		Base Block 01
	0000h	Base Block 00
		<u> </u>

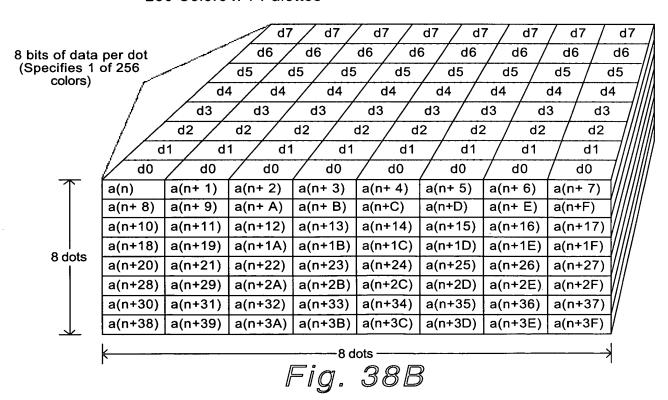
Fig. 37

16 Colors x 16 Palettes

4 bits of dat per dot				
per dot (Specifies 1 c	of 16d3	/ d7 / d3 /	d7 / d3 / d	d7 / d3 / d7
` colors)	d2 /	d6 / d2 /	d6 / d2 / d6	6 / d2 / d6
	d1 d		/	/ d1 / d5 /
	/ d0 / d4	/ d0 / d4	/ d0 / d4	/ d0 / d4 //
1	a(n)	a(n+ 1)	a(n+ 2)	a(n+ 3)
	a(n+ 4)	a(n+ 5)	a(n+ 6)	a(n+ 7)
	a(n+ 8)	a(n+ 9)	a(n+ A)	a(n+ B)
 8 dots	a(n+ C)	a(n+ D)	a(n+ E)	a(n+ F)
o dois	a(n+10)	a(n+11)	a(n+12)	a(n+13)
	a(n+14)	a(n+15)	a(n+16)	a(n+17)
	a(n+18)	a(n+19)	a(n+1A)	a(n+1B)
\downarrow	a(n+1C)	a(n+1D)	a(n+1E)	a(n+1F)
	<u> </u>	80	lots	

Fig. 38A

256 Colors x 1 Palettes



Text BG screen data format

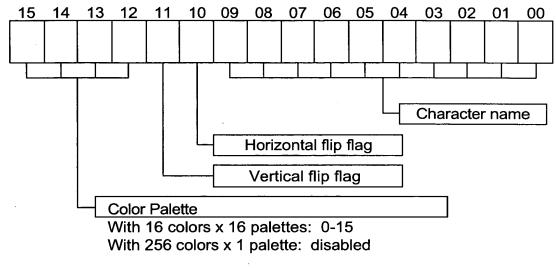


Fig. 39A

Rotation/scaling BG screen data format

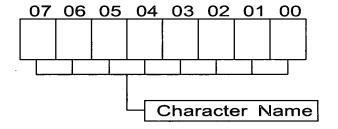
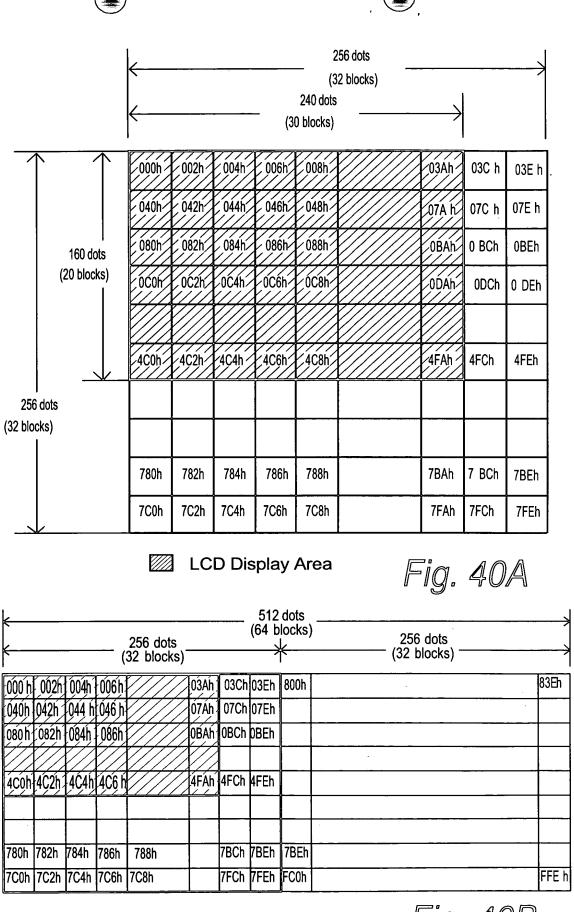


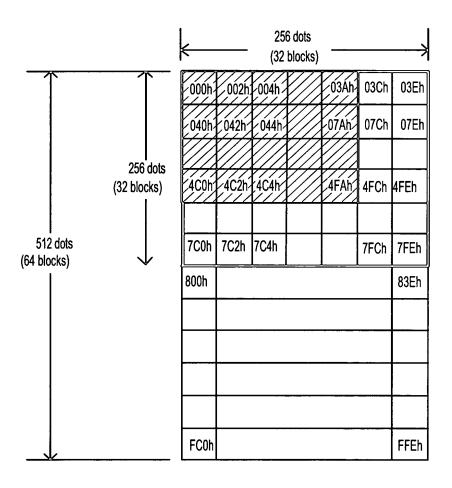
Fig. 39B

256 dots (32 blocks)



LCD Display Area

Fig. 40B



LCD Display Area

Fig. 40C

	←			256 (32 b	dots locks)			dots blocks	256 dots (32 block	s) ———	
\uparrow	000h	002h	004h		03Ah	03Ch	03Eh	800h			83Eh
	040h	042h	044h		07Ah	07Ch	07Eh				
256 dots (32 blocks)									 , ₁ , 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1,		
	4C0h	4C2h	4C4h:		4FAh	4FCh	4FEh				
512 dots	7C0h	7C2h	7C4h			7FCh	7FBh	FC0h	 		FFEh
(64 blocks)	1000h						103Eh	1800h			183Eh
256 dots (32 blocks)					.1				 		
	17C0h			·			17FEh				1FFEh

LCD display area

Fig.40D

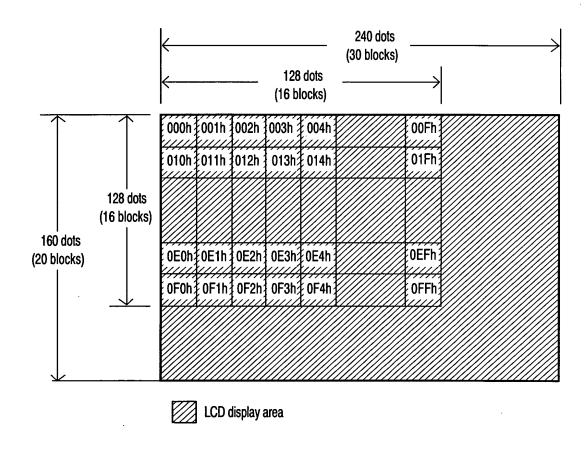
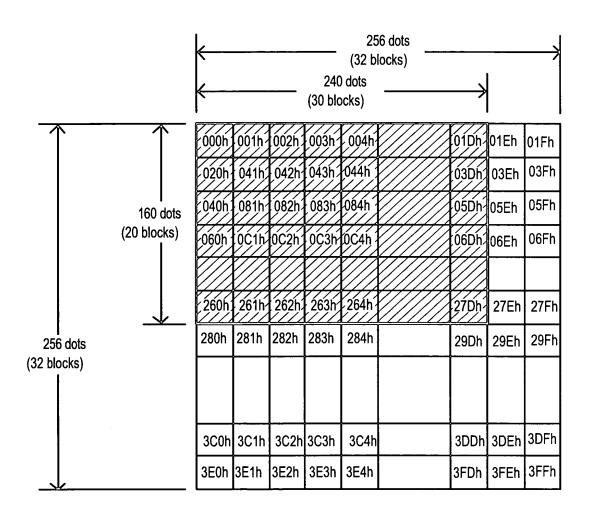


Fig.41A



LCD Display Area

Fig. 41B

不		Æ	ع،	ج	ج, ا	1	ج.	ا ج ا		ī.E	Æ
		1 03Fh	07Fh	- 08Fh	oFFh		4FFh	. 53Fh		n FBFh	FFF
		93Eh	07Eh	OBEh	띮		4FG	53Eh		題	臣
(8)	`										
512 dots (64 blocks)		OEP	05Eh	09Eh	90Eh		4DEh	51Eh	· ·	F9Eh	PDEH
5 		O1Dh	05Dh	9Dh	90		4DDh	51Dh 51Eh		F9Dh	FDDh FDEh
	dots lock	8	94 	8€	8		\$	504h		F84h	FC3h FC4h
	240 dots (30 blocks)	1800	43	83	S		4S3	503h		F83h	된
		002h	42h/	082h 7083F	SCS		\$ \$ \$	502h		F82h	FC2h
		001h 2002h 2003h 2004h	.041h; 042h; 043h	081h	OC1h OC2h OC3h		4Coh 4C1h 4C2h 4C3h	501h		F81h	FC1h FC2h
		000h	040h	080 1	OCO!		4COh	500h		F80h	- - - - -
				— হু	(s) (–		\longrightarrow				
				 160 dots	ploc			I			
				16	(20			512 dots	cks)		
								. q . q	음 		\longrightarrow
		I						, 5 <u>7</u>	9		

Fig.41C

LCD display area

	←			24 (30 bl	0 dots ocks)		1024 do 8 block:			
	000h	001h	.002h	003h	004h	$\angle \angle A$	01Eh	0	7Eh	07Fh
	080h	081h	082h	083h	084h	09Dh	09Eh	 0	FEh	0FFh
	100h	101h	102h	103h	104h	11Dh	11Eh	1	7Eh	17Fh
(20 blocks)	180h	181h	182h	183h	184h	19Dh	19Eh	1	FEh	1FFh
	980h	981h	982h	983h	984h	99Dh	99Eh	9	FEh	9FFh
1024 dots	A00h	A01h	A02h	A03h	A04h	A1Dh	A1Eh	A	7Eh	A7Fh
(128 blocks)										
	3F00h	3F01h	3F02h	3F03h	3F04h	3F1Dh	3F1Eh	3F	7Eh	3F7Fh
	3F80h	3F81h	3 F 82h	3F83h	3F84h	3F9Dh	3F9Eh	3F	FEh	3FFFh

LCD Display Area

Fig. 41D

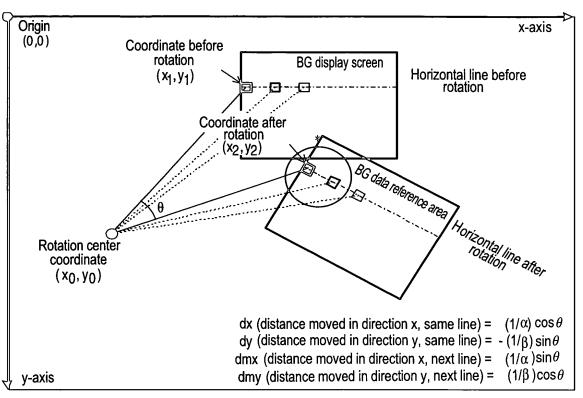
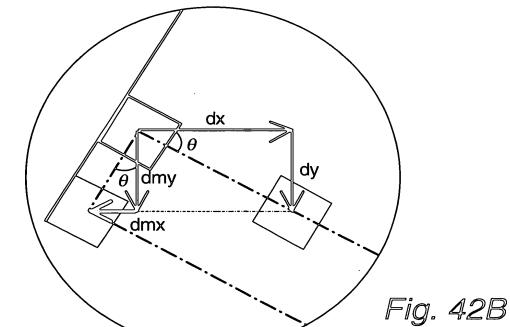
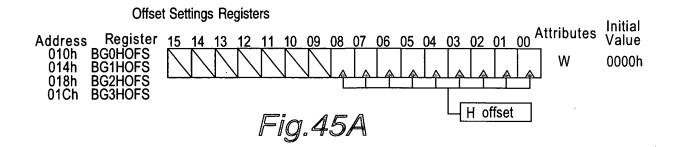


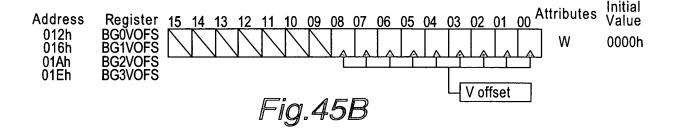
Fig. 42A

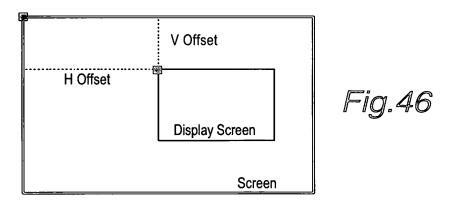
α: Magnification along x-axi β: Magnification along y-axi



Address Register 028h BG2X L 038h BG3X_L Fig.43A	15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00 Attributes X-coordinate of reference starting point (rotation/scaling results) W	Initial Value 0000h
Address Register 02Ah BG2X H 03Ah BG3X_H Fig.43B	15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00 Attributes X-coordinate of reference starting point (rotation/scaling results) W	Initial Value 0000h
Address Register 02Ch BG2Y L 03Ch BG3Y_L Fig.43C	15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00 Attributes Y-coordinate of reference starting point (rotation/scaling results) W	Initial Value 0000h
Address Register 02Eh BG2Y H 03Eh BG3Y_H Fig.43D	15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00 Attributes Y-coordinate of reference starting point (rotation/scaling results) W	Initial Value 0000h
Address Register 020h BG2PA 030h BG3PA	15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00 Attributes dx: distance of movement in x direction along same line A A A A A A A A A A	Initial Value 0100h
Address Register 022h BG2PB 032h BG3PB	15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00 Attributes dmx: distance of movement in x direction along next line \[\lambda \lamb	Initial Value 0000h
Address Register 024h BG2PC 034h BG3PC	15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00 dy: distance of movement in y direction along same line A A A A A A A A A A	Initial Value 0000h
Address Register 026h BG2PD 036h BG3PD	Attributes dmy: distance of movement in y direction along next line \[\lambda \lamb	Initial Value 0100h







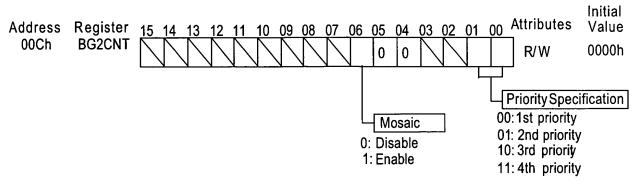


Fig.47

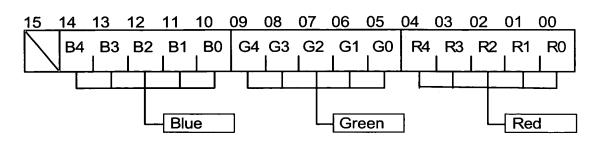


Fig.48A

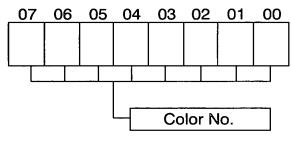


Fig. 48B

	0	1	2	3	4	000	236	237	238	239
0	0h	2h	4h	6h	8h	000	1D8h	1Dah	1DCh	1DEh
1	1E0h	1E2h	1E4h	1E6h	1E8h	000	3B8h	3Bah	3BCh	3BEh
2	3C0h	3C2h	3C4h	3C6h	3C8h	000	598h	59Ah	59Ch	59Eh
3	5A0h	5A2h	5A4h	5A6h	5A8h	000	778h	77Ah	77Ch	7Eh
4	780h	782h	784h	786h	788h	000	958h	95Ah	95Ch	95Eh
156	12480h	12482h	12484h	12486h	12488h	000	12658h	1265Ah	1265Ch	1265Eh
157	12660h	12662h	12664h	12666h	12668h	000	12838h	1283Ah	1283Ch	1283Eh
158	12840h	12842h	12844h	12846h	12848h		12A18h	12A1Ah	12A1Ch	12A1Eh
159	12A20h	12A22h	12A24h	12A26h	12A28h	000	12BF8h	12BFAh	12BFCh	12BFEh

VRAM address (+06000000h)

Frame 0

	0	1	2	3	4	***	236	237	238	239
0	0h	1h	2h	3h	4h	• • •	ECh	EDh	É	EFh
1	F0h	F1h	F2h	F3h	F4h	•••	1DCh	1DDh	1DEh	1DFh
2	1E0h	1E1h	1E2h	1E3h	1E4h	•••	2CCh	2CDh	2CEh	2CFh
3	2D0h	2D1h	2D2h	2D3h	2D4h	•••	3BCh	3BDh	3BEh	3BFh
4	3C0h	3C1h	3C2h	3C3h	3C4h	• • •	4ACh	4ADh	4AEh	4AFh
						l				
156	9240h	9241h	9242h	9243h	9244h	•••	932Ch	932Dh	932Eh	932Fh
157	9330h	9331h	9332h	9333h	9334h	***	941Ch	941Dh	941Eh	941Fh
158	9420h	9421h	9422h	9423h	9424h	•••	950Ch	950Dh	950Eh	950Fh
159	9510h	9511h	9512h	9513h	9514h	• • •	95FCh	95FDh	95FEh	95FFh

VRAM address (+06000000h)

Fig. 50A

Frame 1

	0	1	2	3	4	•••	236	237	238	239
0	A000h	A001h	A002h	A003h	A004h		A0ECh	A0EDh	A0EEh	A0EFh
1	A0F0h	A0F1h	A0F2h	A0F3h	A0F4h	•••	A1DCh	A1DDh	A1DEh	A1DFh
2	A1E0h	A1E1h	A1E2h	A1E3h	A1E4h		A2CCh	A2CDh	A2CEh	A2CFh
3	A2D0h	A 2D1h	A2D2h	A 2D3h	A2D4h		A3BCh	A3BDh	A3BEh	A3BFh
4	A3C0h	A 3C1h	A3C2h	A 3C3h	A3C4h		A4ACh	A4ADh	A4AEh	A 4AFh
1	1			_						
156	13240h	13241h	13242h	13243h	13244h	• • •	1332Ch	1332Dh	1332Eh	1332Fh
157	13330h	13331h	13332h	13333h	13334h	•••	1341Ch	1341Dh	1341Eh	1341Fh
158	13420h	13421h	13422h	13423h	13424h	•••	1350Ch	1350Dh	1350Eh	1350Fh
159	13510h	13511h	13512h	13513h	13514h	•••	135FCh	135FDh	135FEh	135FFh

VRAM address (+06000000h)

Fig. 50B

Fig. 51A

Frame 0

	0	1	2	3	4	•	156	157	158	159			
0	0h	2h	4h	6h	8h		138h	13Ah	13Ch	13Eh			
1	140h	142h	144h	146h	148h	•	298h	29Ah	29Ch	29Eh			
2	2A0h	2A2h	2A4h	2A6h	2A8h	•••	3B8h	3BAh	3BCh	3BEh			
3	3C0h	3C2h	3C4h	3C6h	3C8h		4F8h	4FAh	4FCh	4FEh			
4	500h	502h	504h	506h	508h	• • •	638h	63Ah	63Ch	63Eh			
124	9B00h	9B02h	9B04h	9B06h	9B08h	• • •	9C38h	9C3Ah	9C3Ch	9C3Eh			
125	9C40h	9C42h	9C44h	9C46h	9C48h	• • •	9D78h	9D7Ah	9D7Ch	9D7Eh			
126	9D80h	9D82h	9D84h	9D86h	9D88h		9EB8h	9EBAh	9EBCh	9EBEh			
127	9EC0h	9EC2h	9EC4h	9EC6h	9EC8h		9FF8h	9FFAh	9FFCh	9FFEh			

VRAM Address (+06000000h)

Fig. 51B

Frame 1

	0	1	2	3	4		156	157	158	159
0	A000h	A002h	A004h	A006h	A008h	• • •	A138h	A13Ah	A13Ch	A13Eh
1	A140h	A142h	A144h	A146h	A148h	• • •	A298h	A29Ah	A29Ch	A29Eh
2	A2A0h	A2A2h	A2A4h	A2A6h	A2A8h	• • •	A3B8h	A3BAh	A3BCh	A3BEh
3	A3C0h	A3C2h	A3C4h	A3C6h	A3C8h	•	A4F8h	A4FAh	A4FCh	A4FEh
4	A500h	A502h	A504h	A506h	A508h	•••	A638h	A63Ah	A63Ch	A63Eh
124	13B00h	13B02h	13B04h	13B06h	13B08h	•••	13C38h	13C3Ah	13C3Ch	13C3Eh
125	13C40h	13C42h	13C44h	13C46h	13C48h		13D78h	13D7Ah	13D7Ch	13D7Eh
126	13D80h	13D82h	13D84h	13D86h	13D88h		13EB8h	13EBAh	13EBCh	13EBEh
127	13EC0h	13EC2h	13EC4h	13EC6h	13EC8h		13FF8h	13FFAh	13FFCh	13FFEh

VRAM address (+06000000h)

		8x16 dots		·	<u></u>	(256 colors/16 palettes)							,,
	01Fh	RS	05Fh	07Eh 07Fh	95F	OBFh	ODBH ODCH ODDH ODEH ODFH	0FFh	11Fh	13Fh	15Fh	17Fh	
	01Eh		05Eh	07Eh	09Eh	OBEN	90 EF	0FEh	11Eh	13Eh	15Eh	17Eh	
	01Ch 01Dh		1050 J	07Ch 07Dh	4080 1080	NOBO!	90	0FDh	11Ch 11Dh	13Dh	15Dh	17Dh	
			05Ch		(3CF)	OBCh OBCh	900	0FCh	11Ch	13Ch	15Ch	17Ch	
	01Bh	03Bh	UBS0	07Bh	09Bh	488 0	чвао	0FBh	11Bh	13Bh	15Bh	17Bh	
(s													
Basic Character 8x8 dots (16 colors/16 palettes)	1800	028h	048h	068h	088h	0A8h	0C8h	0E8h	108h	128h	148h	168h	
s Char x8 do rs/16	100 2017 2017	(027)	047h	067h	.087h	OA7h	UZOO-	OE7h	107h	127h	147h	15/ 167h	
Basid 8 6 colo	1900	026h	046h	066h	086h	OAGH	1900 1900	0E6h	106h	126h	146r	199	
1)	005h	025h	045h	065h	085h	0A5h	OCSh.	0E5h	105h	125h	145h	163	
	004h	024h	044h	064h	084h	OAAh	ocah	OE4h	104h	124h	4	\$	
	(S)	\ <u>\</u>	.043h	.063h	083h	0A3h	OC3h	0E3h	103h	123h	43	-15 -15 -15 -15 -15 -15 -15 -15 -15 -15	
	1200 1200	420	042h	062h	.082h	0A2h	OC2h	0E2h	102h	12h	142h	- 6 2h	
	Sale Ale	18/ 18/	041h	061h	081h	10A1h	0C1h 0C2h	OETH	1011	12/	14. 14.	16th	
		No.	940h	000	080h 081h	OAOh	COL	OEO!	100	12g	\$	\$	
	32x32 dots	(10 colois) to parettes)			64x64 dots (15 colors 11 c	(10 colois/ 10 palettes)							

Fig. 52

Character mapping area (character no. in hexadecimal notation)

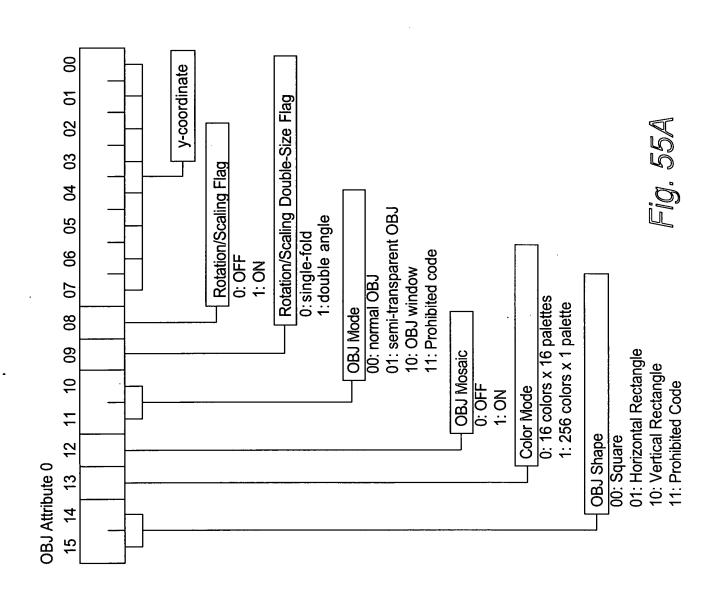
Character name

								<u>↓</u>							_
With OBJ Character Display		8	ĸ		1	1 n+2 n+3 n+4 n+5 n+6 n+7	9 n+10 n+11 n+12 n+13 n+14 n+15	17 n+18 n+19 n+20 n+21 n+22 n+23	25 n+26 n+27 n+28 n+29 n+30 n+31	33 n+34 n+35 n+36 n+37 n+38 n+39	n+40 n+41 n+42 n+43 n+44 n+45 n+46 n+47	n+48 n+49 n+50 n+51 n+52 n+53 n+54 n+55	57 n+58 n+59 n+60 n+61 n+62 n+63		
Basic Character Unit Image	1+U U L+U	n+2 n+3	n+4 n+5	1 basic character n+6 n+7 64 bytes		n+63 n n+1	n+62 n+9	n+16 n+17	n+24 n+25	n+32 n+33	n+2 n+40 n+40	n+1	n 1 basic character n+56 n+57		n Character name
VRAM OBJ Character Storage Area		16 x 32-dot character	(256 colors x 1 palette format)		8 x 8-dot character (16 colors x 16 palette format)				64 x 64-dot character	(16 colors x 16 palette format)				16 x 16-dot character (256 colors x 1 palette format)	
	p20h			920h	91Fh 900h	8FF			-				100	0FFh 0000	<u></u>

Fig. 53

		OAIVI
070003FEh	Rotatio	n/Scaling Parameter PD-31
		Attribute 2
	OBJ127	Attribute 1
		Attribute 0
		•
		• • •
		: :
	Rotatio	n/Scaling Parameter PB-0
		Attribute 2
	OBJ1	Attribute 1
		Attribute 0
	Rotatio	n/Scaling Parameter PA-0
		Attribute 2
	OBJ0	Attribute 1
07000000h		Attribute 0
		——————————————————————————————————————

Fig. 54



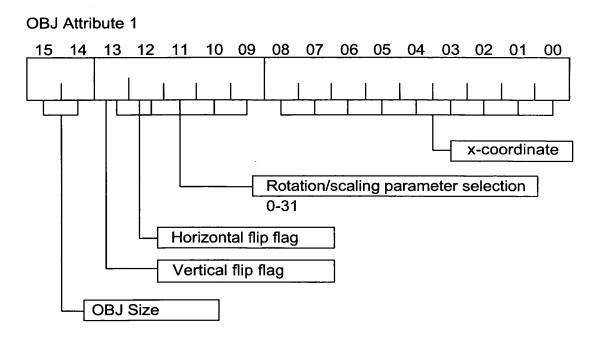


Fig. 55B

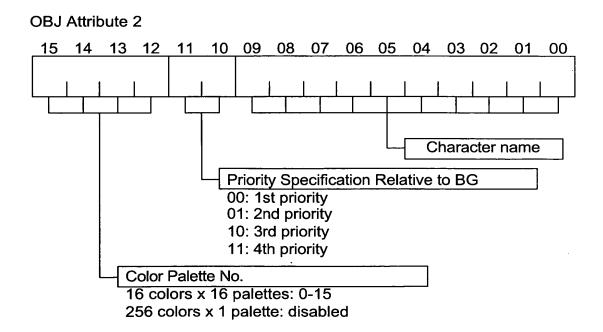
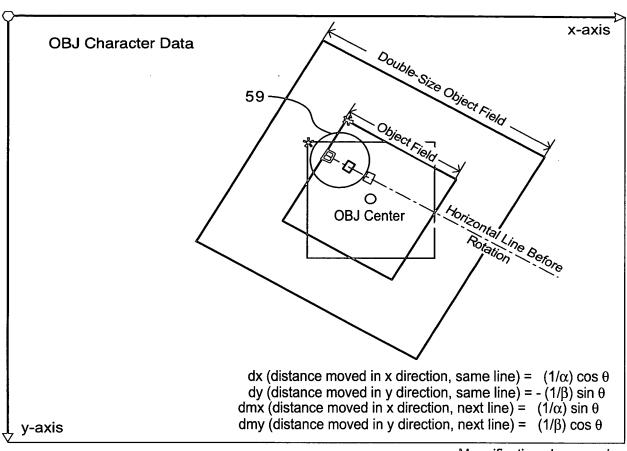


Fig. 55C

Rotation Display	©	Rotation Display (Double-Size object field)	
Normal Display		Magnified (x2) Display (Double-Size object field)	O
			·

	\$ \$		32x64	
OBJ Size	32x32 32x32	32x16	16x32	Prohibited Code
001 001	16×16	32x8	8%37 	Prohibi
00	& & & & & & & & & & & & & & & & & & &	Alorizontal Rectangle (m)	Vertical Rectangle	
OBU		2 Honstae Allendring H		

Fig. 57



α: Magnification along x-axis β: Magnification along y-axis

Fig. 58A

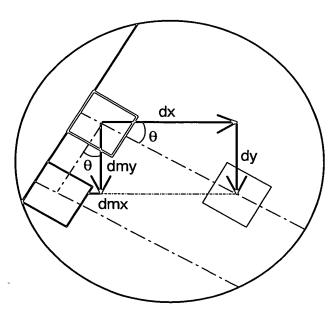
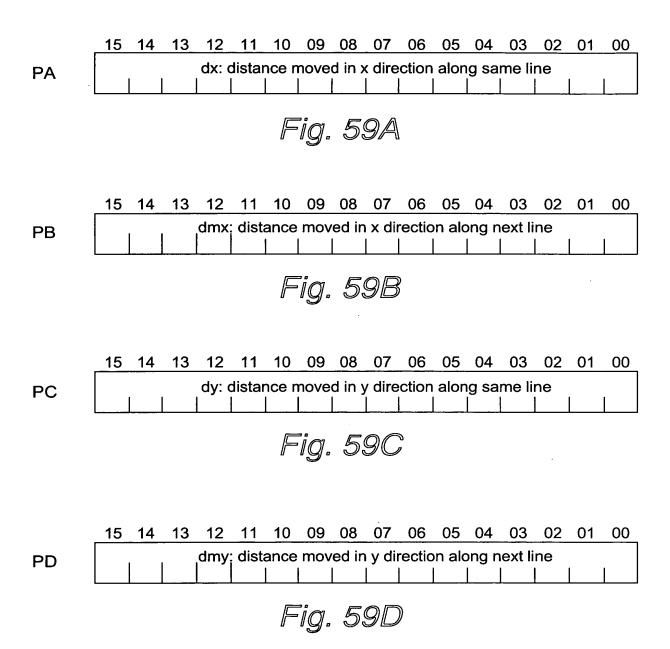


Fig. 58B



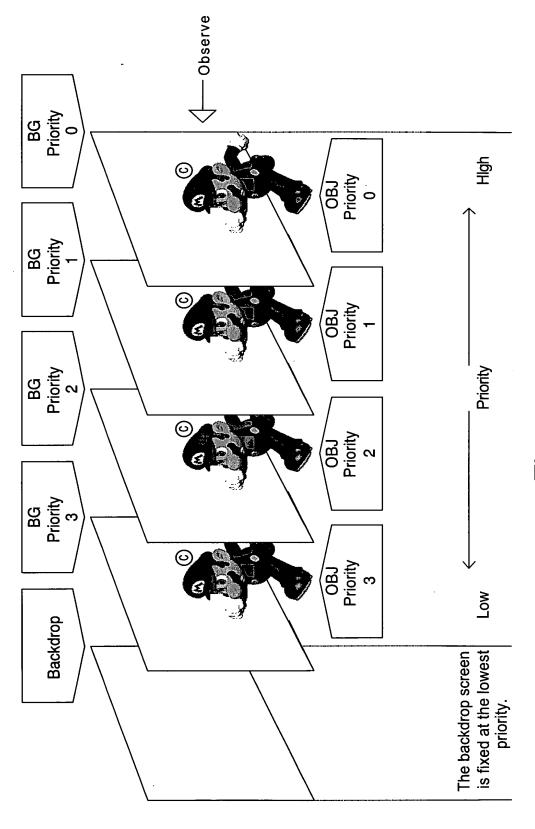


Fig. 60

Palette RAM

050003FFh	OBJ Palette RAM 512 bytes
05000200h 050001FFh	
	BG Palette RAM 512 bytes
05000000h	

Fig. 61

16 Colors x 16 Palettes

	Color 0	or 1	Color 2	Color 3				r 13	r 14	r 15						
	Col	Color 1	Col	Col				Color 13	Color 14	Color 15	-					
				·												
Palette RAM	Palette 0	Palette 1	Palette 2	Palette 3	Palette 4	Palette 5	Palette 6	Palette 7	Palette 8	Palette 9	Palette 10	Palette 11	Palette 12	Palette 13	Palette 14	Palette 15

256 Colors x 1 Palette

Palette RAM

Color 0	Color 1	Color 2	Color 3	Color 4		 	 	 	Color 252	Color 253	Color 254	Color 255
						Palette 0						

Fig. 62B

Fig. 62A

Color Data Format

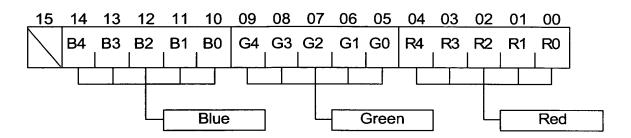


Fig. 63

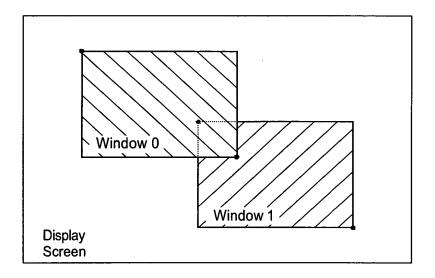


Fig. 64

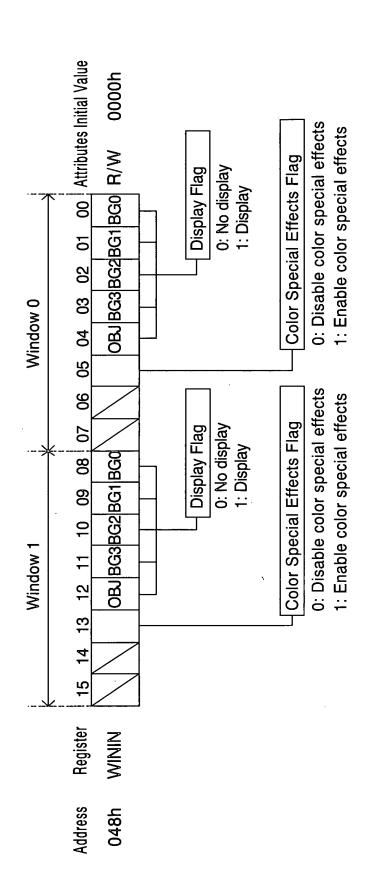


Fig. 65

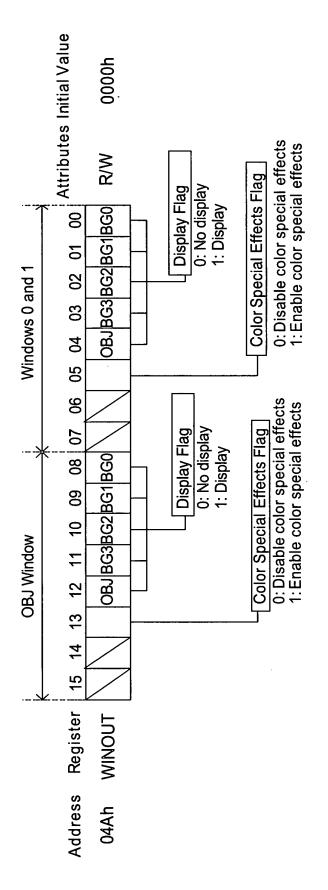


Fig. 66

(

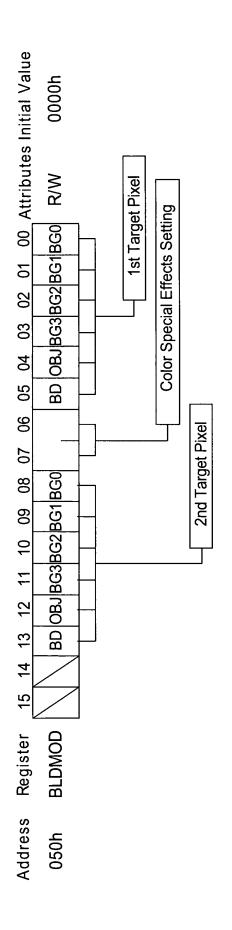
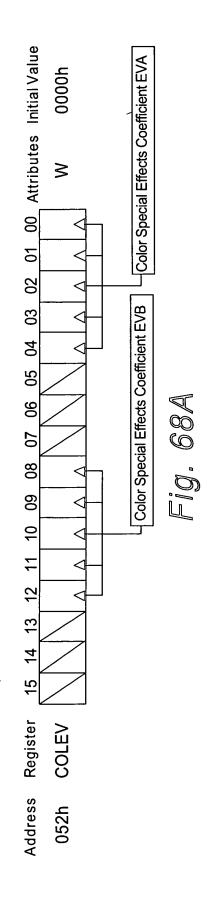


Fig. 67



03 02 01 00 Attributes Initial Value - Color Special Effects Coefficient EVY 0000h ≥ 8 02 Fig. 68B 90 08 07 60 9 12 11 14 13 15 Address Register COLY 054h

EVB, EVY Coeff. EVA, EVB, EVY O<										
EVB, EVY 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Coeff.	8/16	9/16	10/16	11/16	12/16	13/16	14/16	15/16	16/16
EVB, EVY Coeff. EVA, EVB 0 0 0 1 0 0 0 1 1/16 0 1 0 0 1 0 1 0 1 0 0 1 1 3/16 0 1 1 1 0 0 4/16 0 1 1 1 0 1 5/16 0 1 1 1 1 1 7/16 0 1 1 1 1 1 7/16 0 1 1 1 1 1 7/16 0 1 1		0	l	0	1	0	1	0	1	X
EVB, EVY 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0	EVY	0	0	l	l	0	0	l	l	Χ
EVB, EVY 0 0 0 0 0 1 0 0 1 1/16 0 1 0 1 0 2/16 0 1 1 0 0 4/16 0 1 1 0 0 4/16 0 1 1 1 0 6/16 0 1 1 1 1 7/16 0 1	EVB	0	0	0	0	1	1	1	1	X
EVB, EVY Coeff. 0 0 0 0 0 0 1 1/16 0 1 0 2/16 1 0 0 4/16 1 1 0 0 6/16 1 1 1 7/16	EVA	1	l	1	ļ	1	1	1	1	×
EVB, EVY 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1		0	0	0	0	0	0	0	0	1
EVB, EVY 0 0 0 1 1 1 1 0 0 0 1 1 1 1 1 1 1 1 1		0	1/16	2/16	3/16	4/16	5/16	6/16	7/16	
	EVA, EVB, EVY	0	l	0	1	0	1	0	1	
		0	0	Į	l	0	0	1	1	
		0	0	0	0	1	1	1	1	
		0	0	0	0	0	0	0	0	
000000		0	0	0	0	0	0	0	0	

Fig. 69

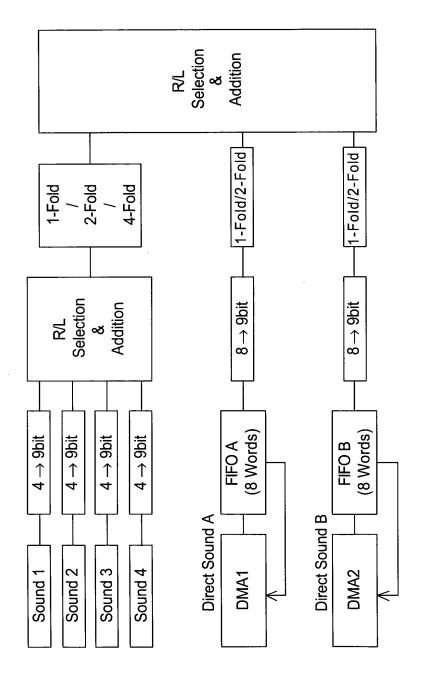


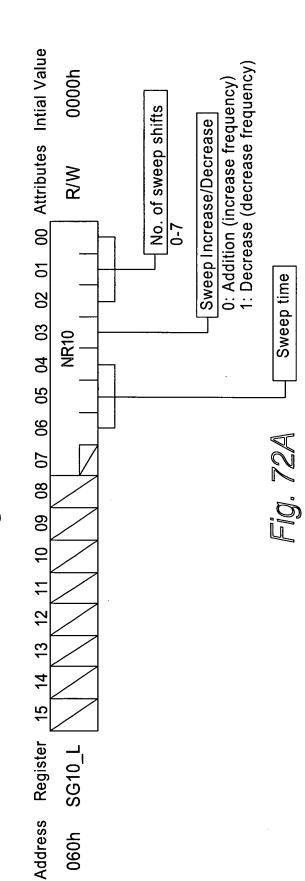
Fig. 70

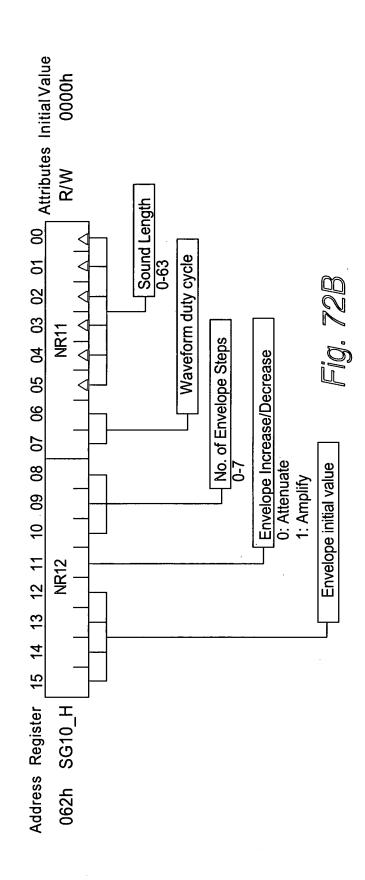
15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00 Attributes Initial Value ≥ Sound Data 0 Sound Data 1 SGFIFOB_L Register SGFIFOA_L Address 0A0h 0A4h

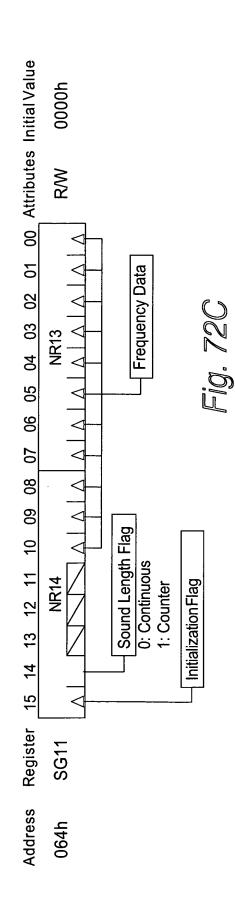
Fig. 71A

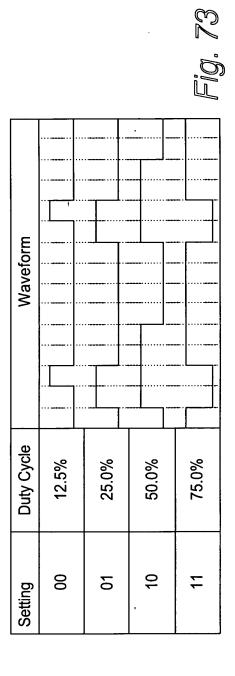
15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00 Attributes Initial Value ≥ Sound Data 2 Sound Data 3 SGFIFOB_H SGFIFOA_H Register Address 0A2h 0A6h

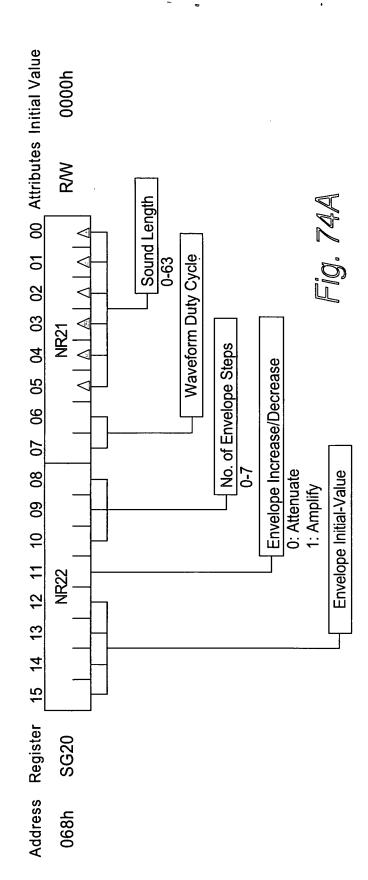
Fig. 71B

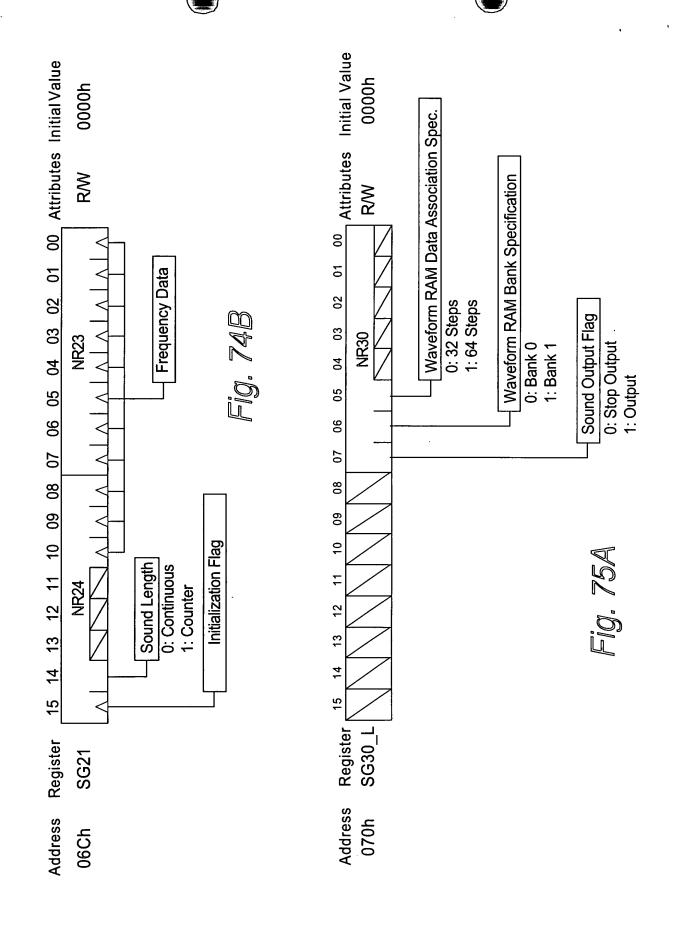


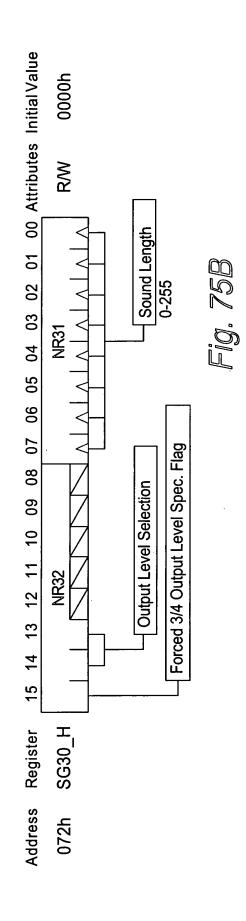












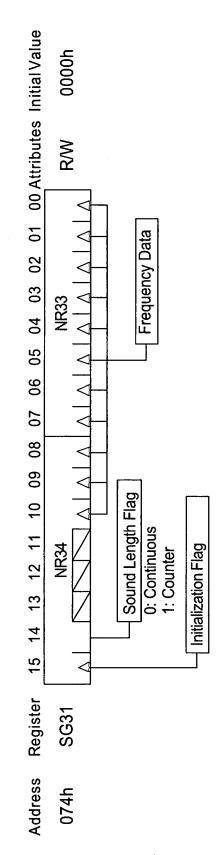


Fig. 75C

Attributes Initial Value	R/W -		3 12 11 10 09 08 07 06 05 04 03 02 01 00 Attributes Initial Value	R.W.
8			8	
9	φ		9	Step 5
8	Step 1		02	Ste
ဗ			03	
8			8	
02	p 0		05	Step 4
90	Step 0		90	Ste
6	.	192	07	
8		Fig. 76A	80	
15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00	Step 3		60	Step 7
9	Ste		10	Ste
=			7	
12	· 		12	_
13	Step 2		13	9 d
4	Ste		15 14 1	Step (
15			15	
Register	090h SGWR0_L		Address Register	092h SGWR0_H
Address	4060		Address	092h

Fig. 76B

Fig. 76C

Fig. 760

Attributes Initial Value R/W -	Attributes Initial Value	Attributes Initial Value	Attributes Initial Value	RW -
15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00 Step 18 Step 19 Step 16 Step 17	15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00 Step 22 Step 23 Step 20 Step 21	15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00 Step 26 Step 27 Step 24 Step 25	Fig. 76G	Step 30 Step 31 Step 28 Step 29
Address Register 098h SGWR2_L	Address Register 09Ah SGWR2_H	Address Register 09Ch SGWR3_L	מיסיבים מיסיבים	09Eh SGWR3_H

Fig. 76H

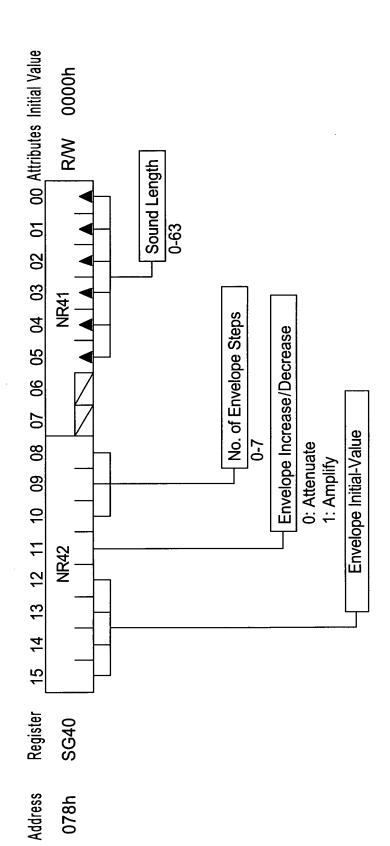


Fig. 77A

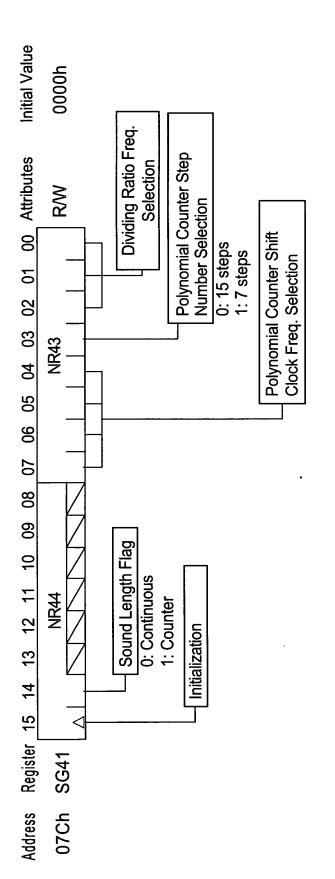


Fig. 77B

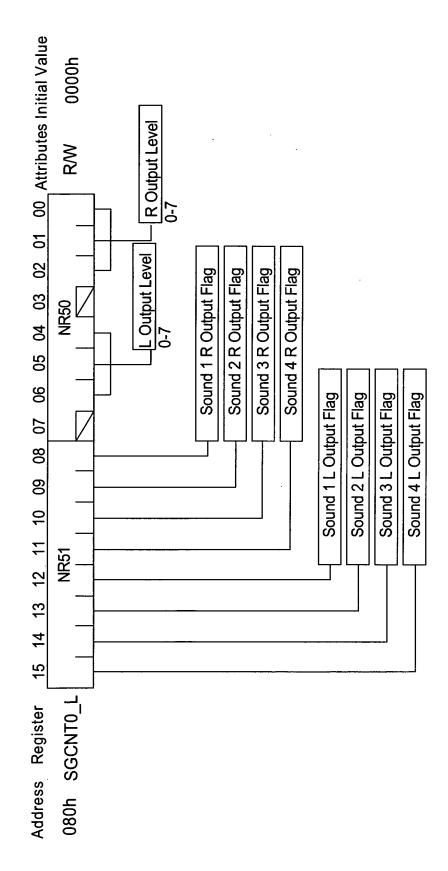


Fig. 78A

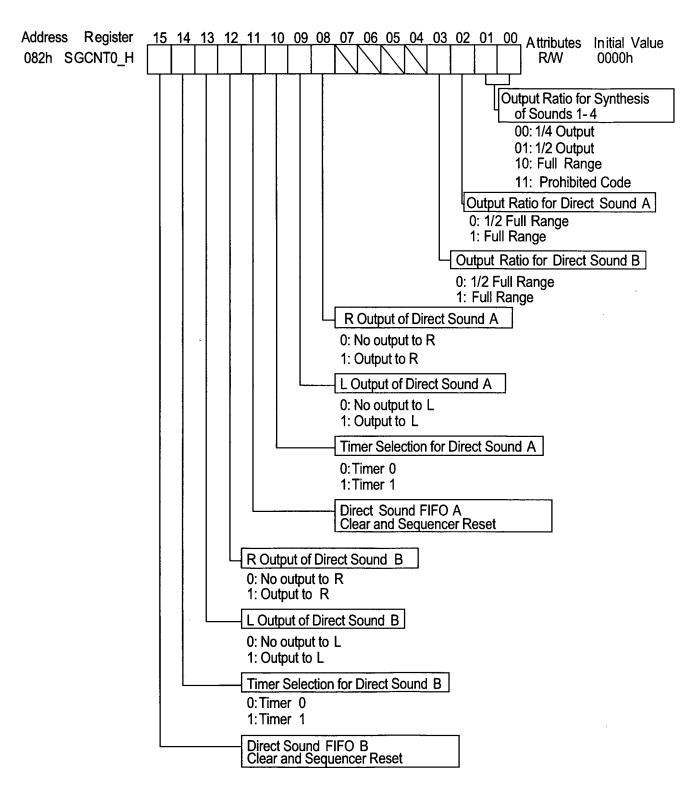


Fig. 78B

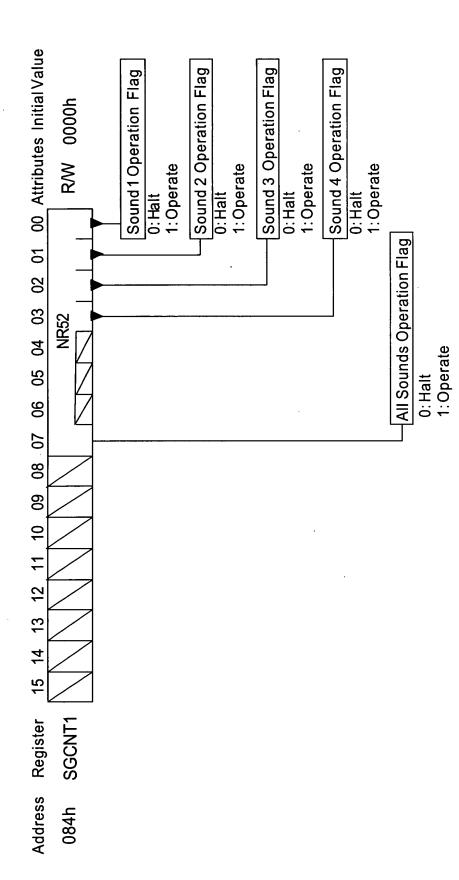
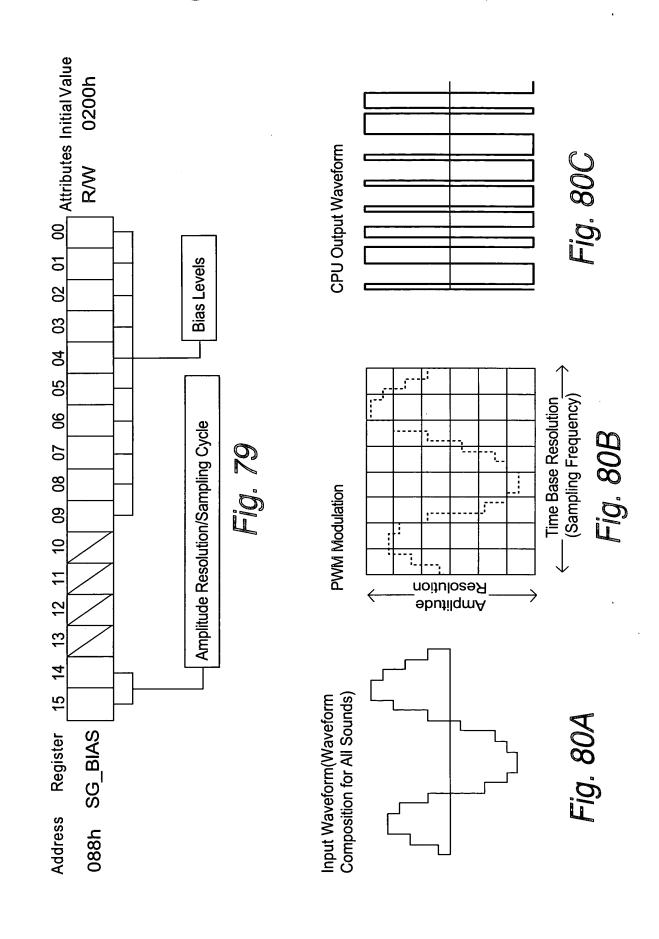


Fig. 78C



1) Timer Setting

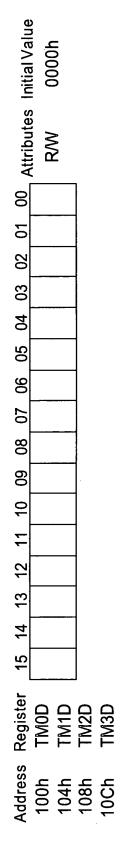


Fig. 81A

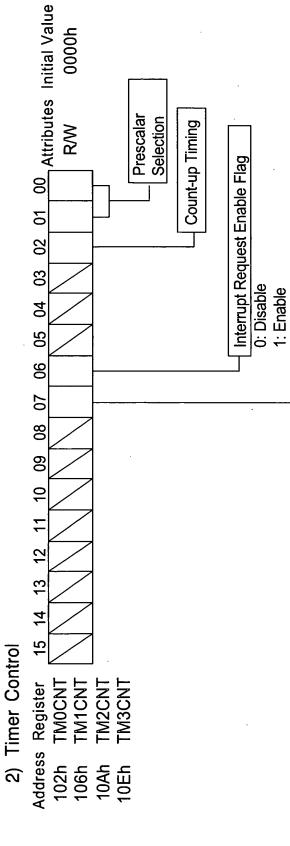
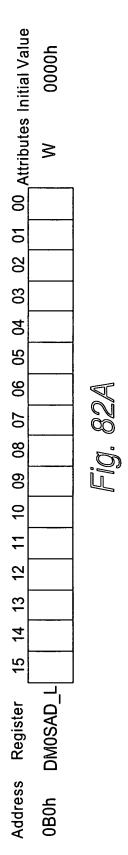


Fig. 81B

Timer Operation Flag

0: Disable 1: Enable

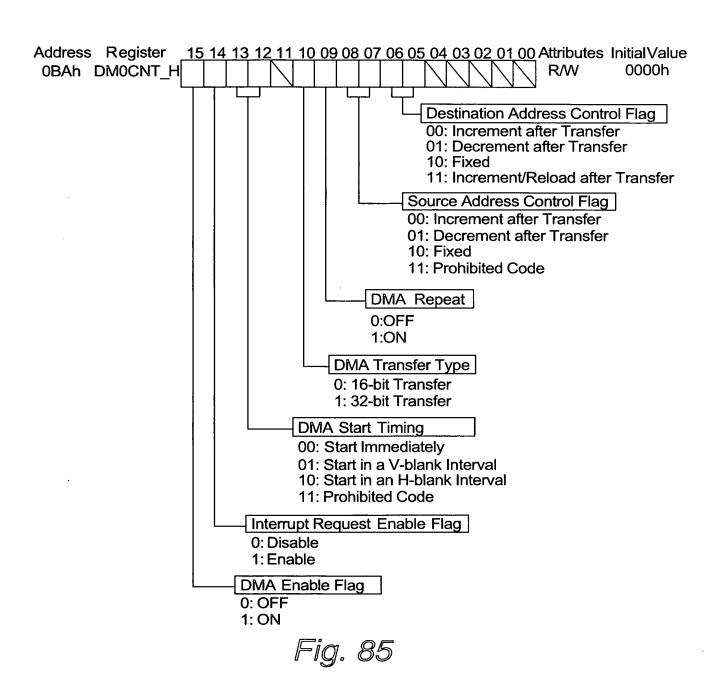


02 01 00 Attributes Initial Value 0000h ≥ 03 04 02 09 08 07 06 11 10 12 13 14 15 0B2h DM0SAD_H Register Address

Fig. 82B

0000h ≥ Fig. 83B DM0DAD_H Address Register 0B6h

00 Attributes Initial Value 0000h ≥ 02 01 03 05 04 90 Fig. 84 10 09 08 07 = 12 13 4 DM0CNT_L Register Address 0B8h



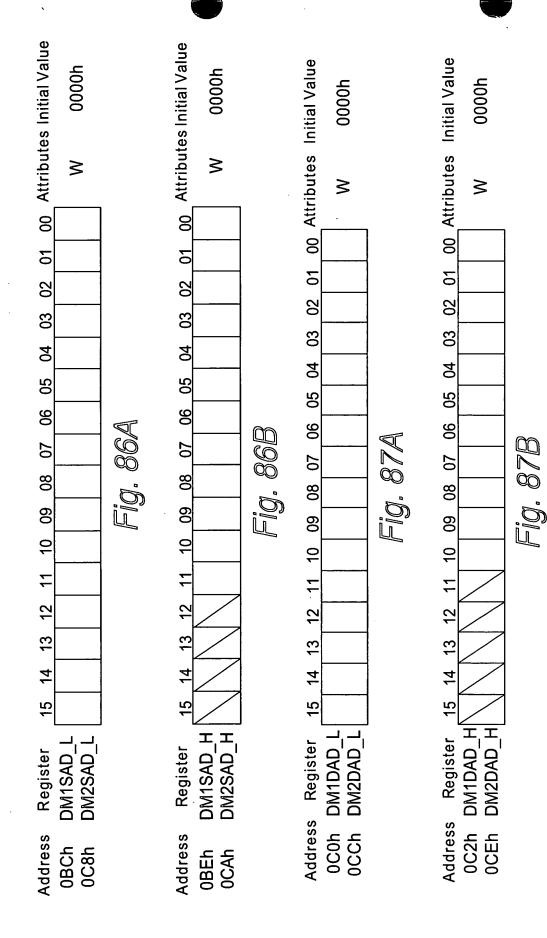


Fig. 88

01 00 Attributes Initial Value

05

03

8

05

9

07

8

10 09

-

12

13

4

15

Address

DM2CNT_L

OD0h

Register DM1CNT

0C4h

0000h

≥

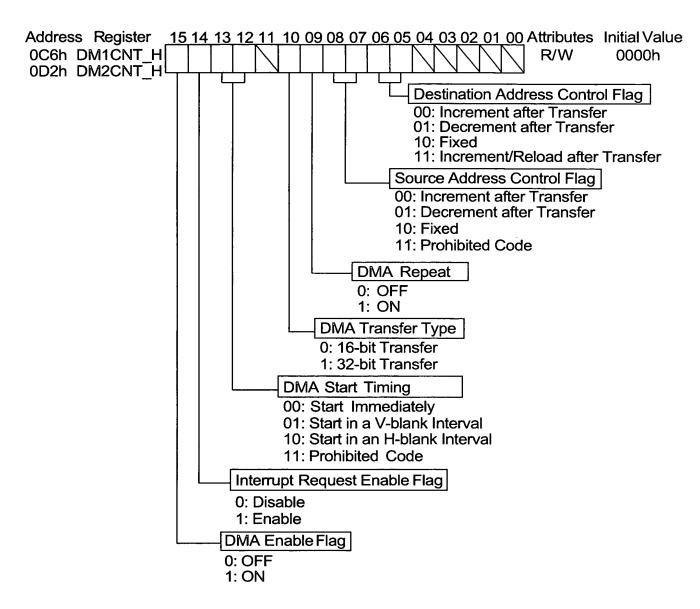
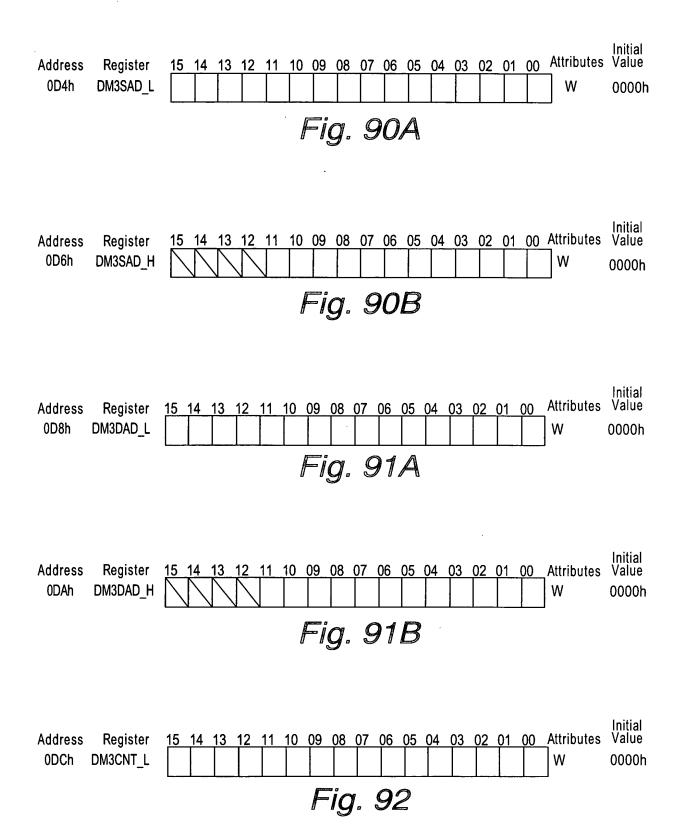
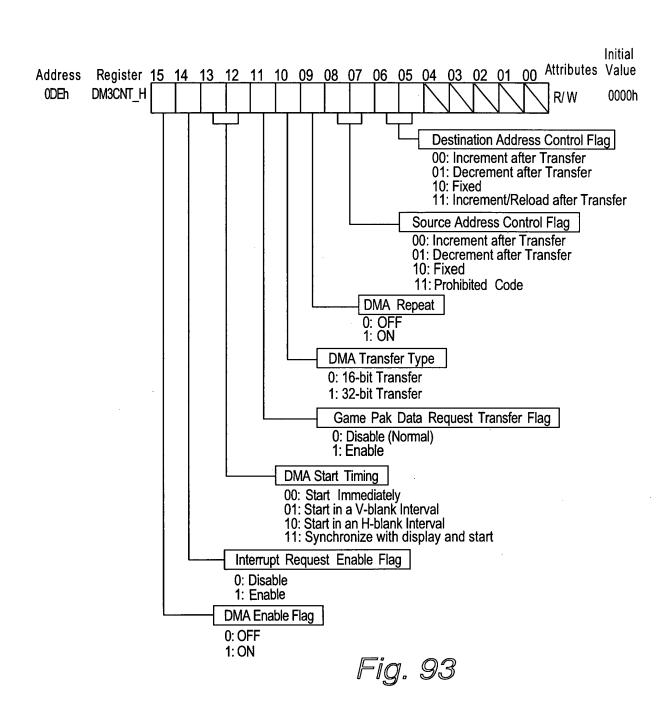
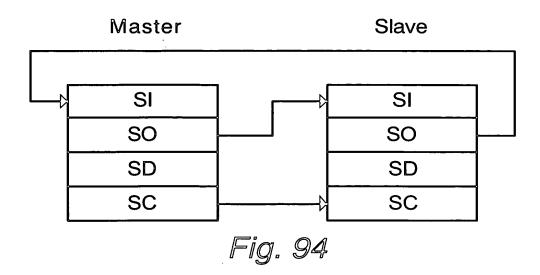


Fig. 89







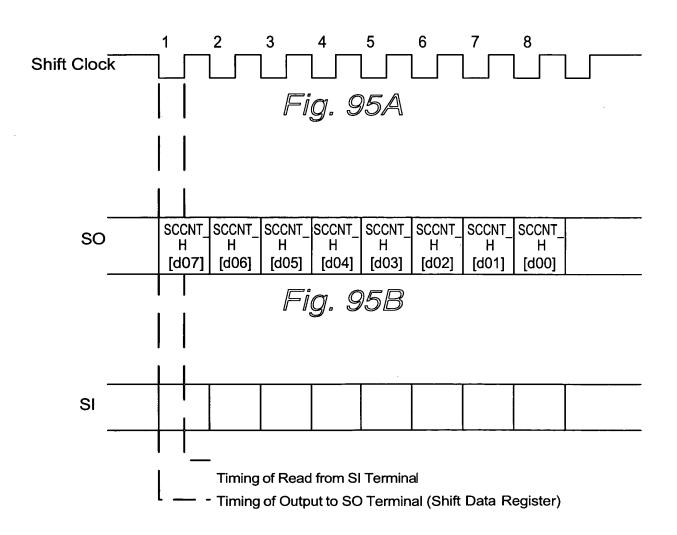
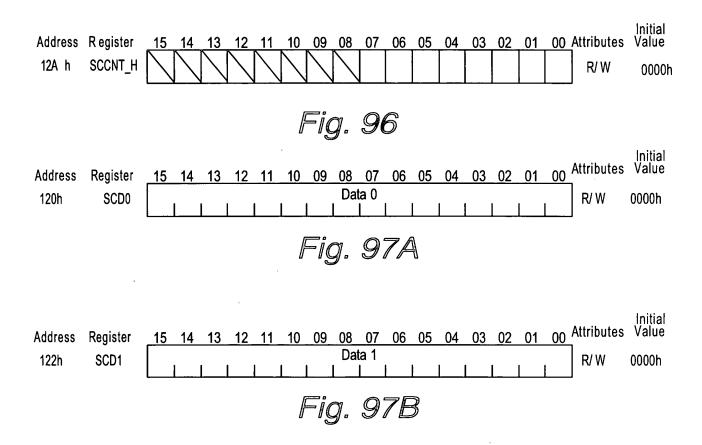
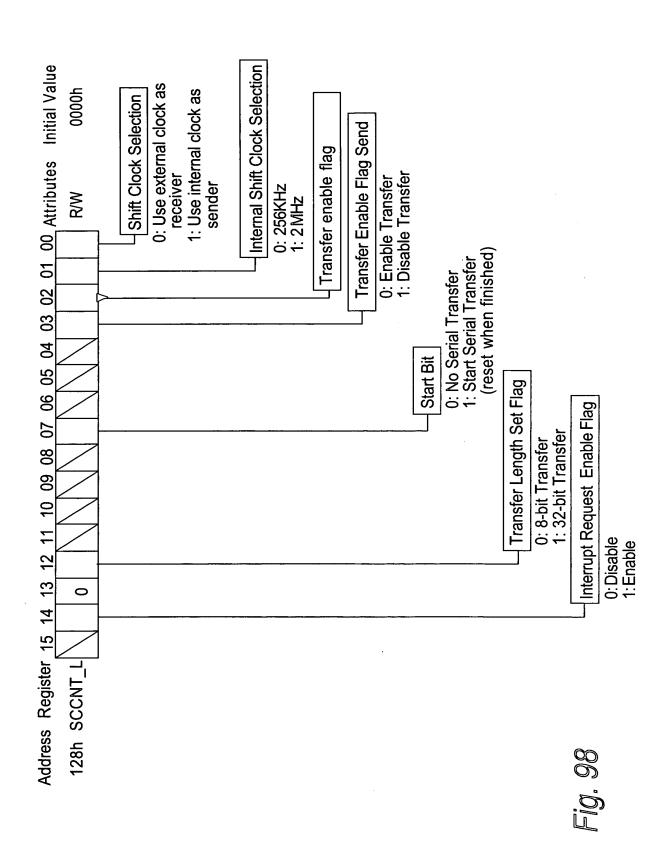
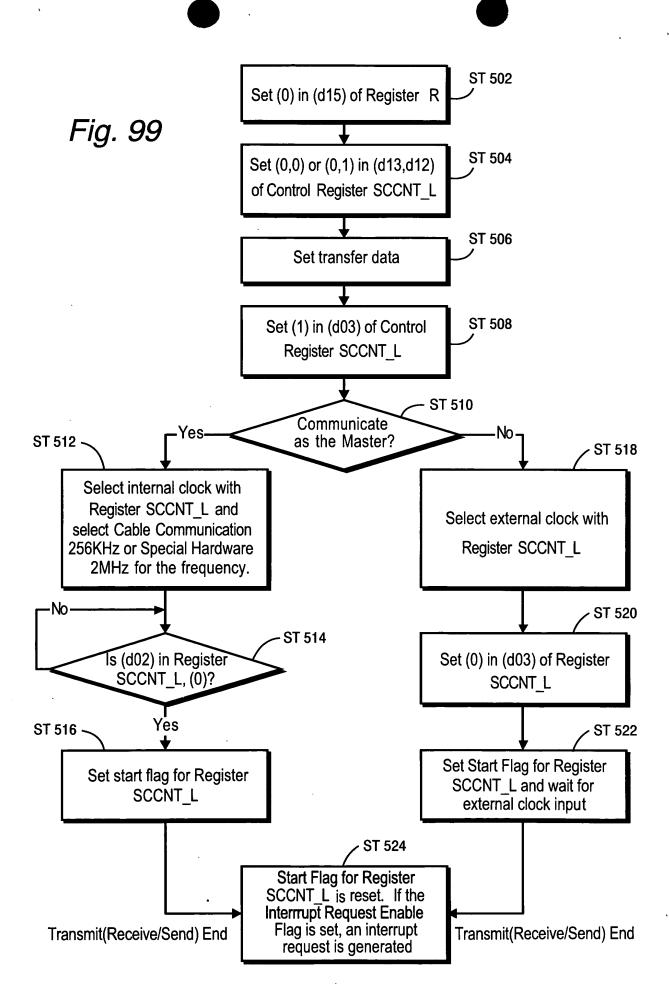


Fig. 95C







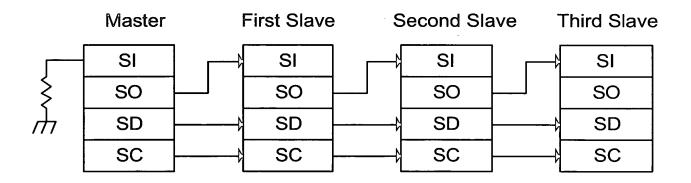
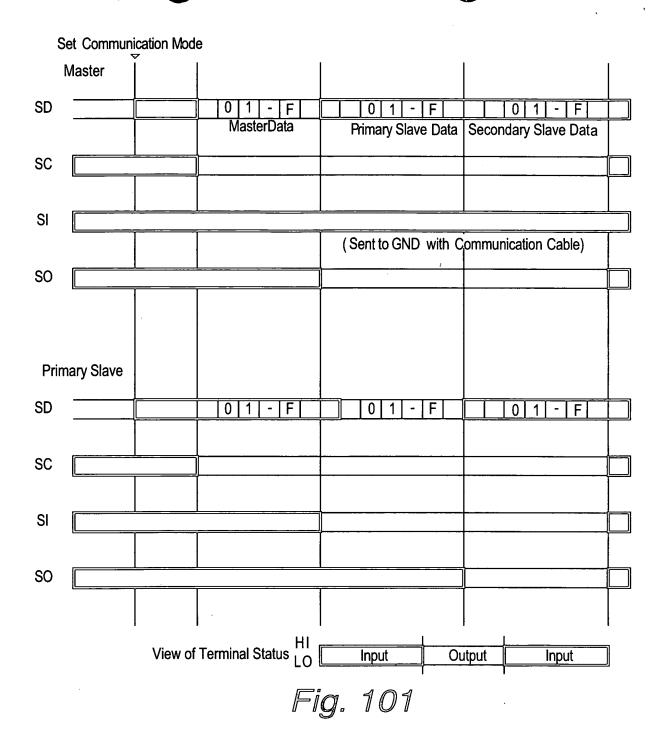
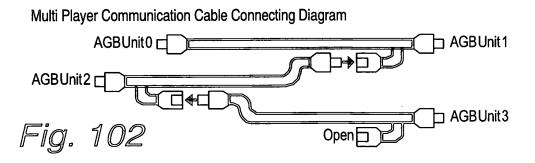
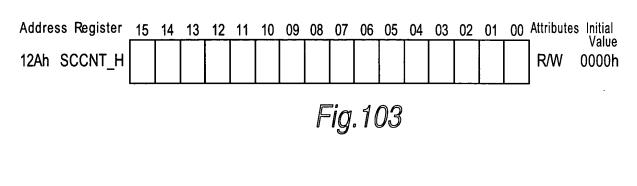
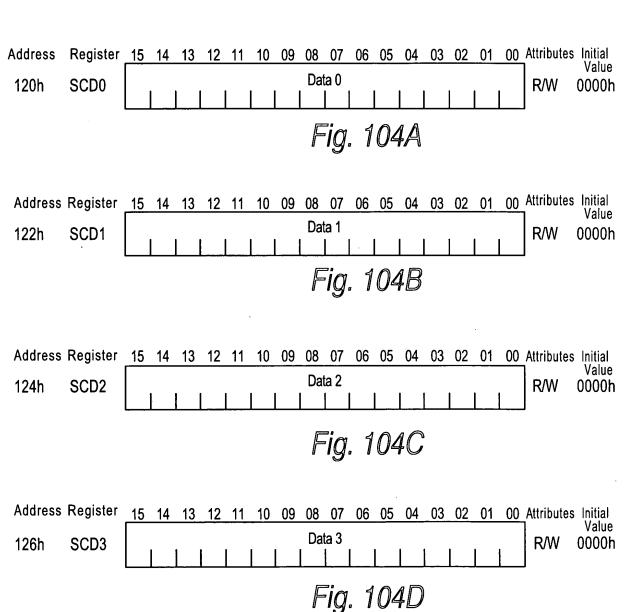


Fig. 100









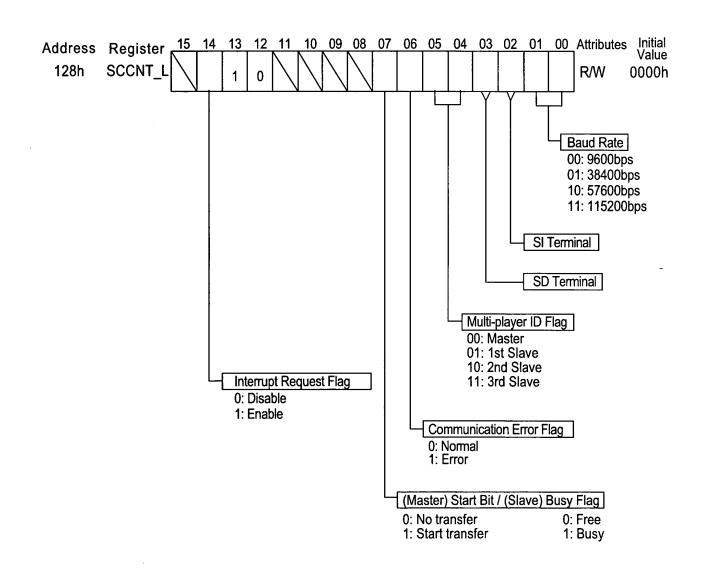
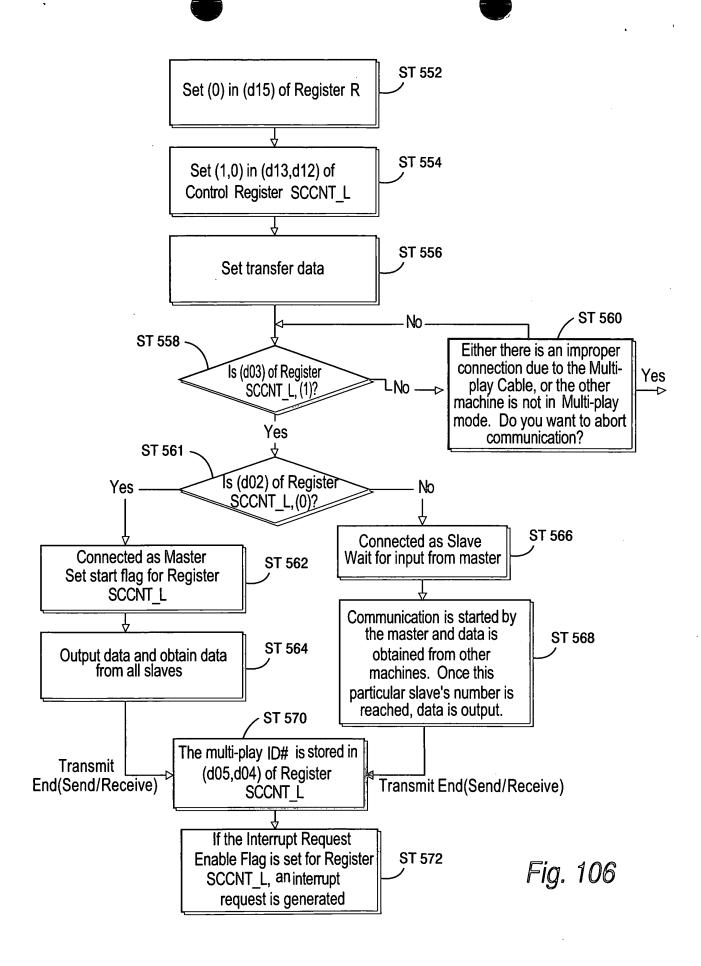


Fig. 105



UART Communication

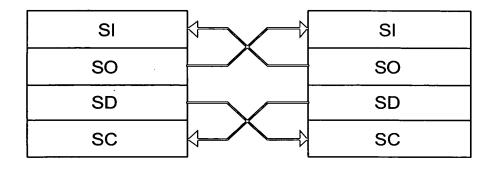


Fig. 107

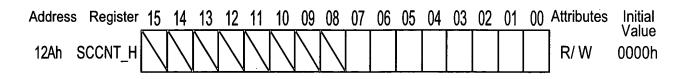
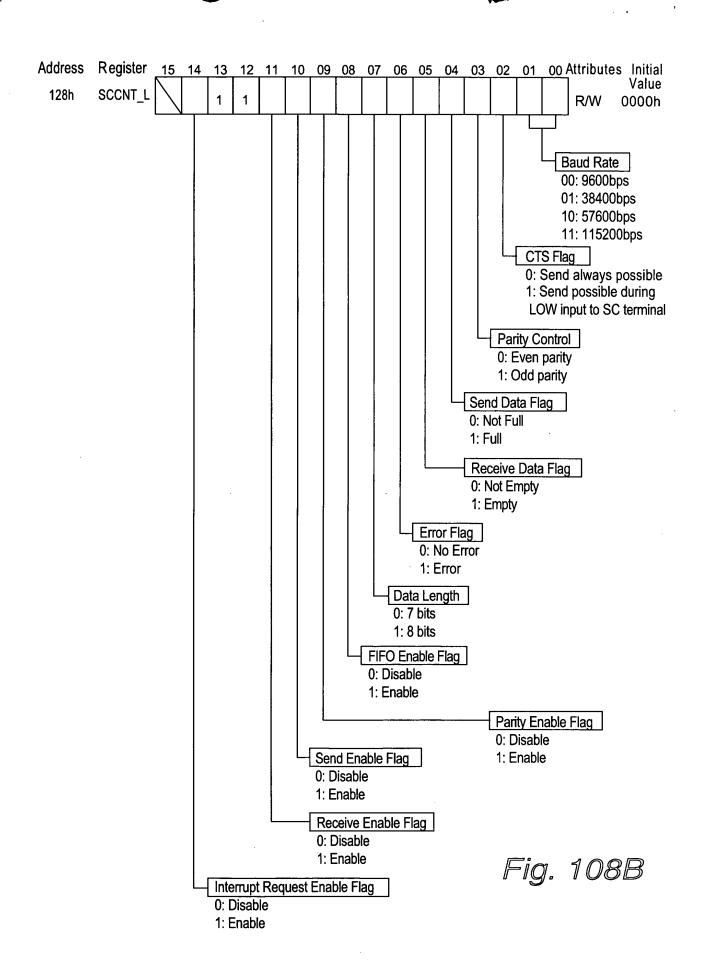


Fig. 108A



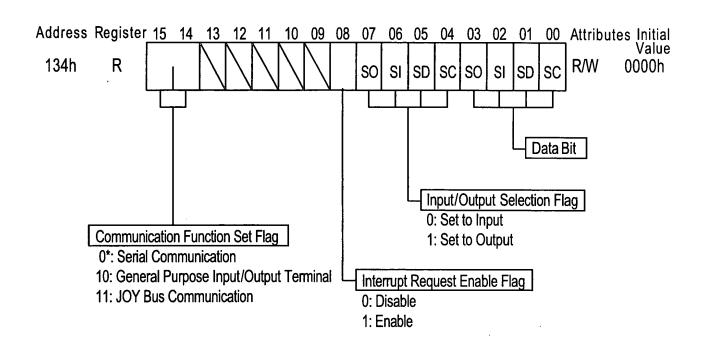


Fig. 109

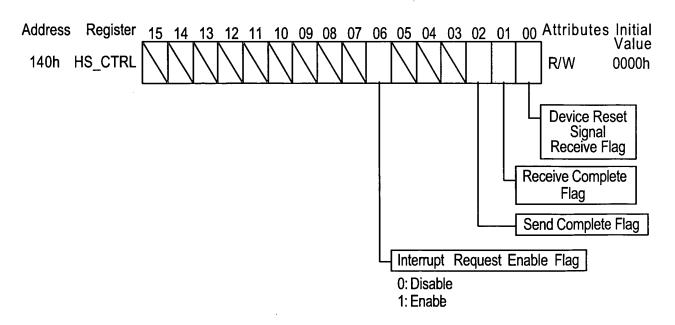
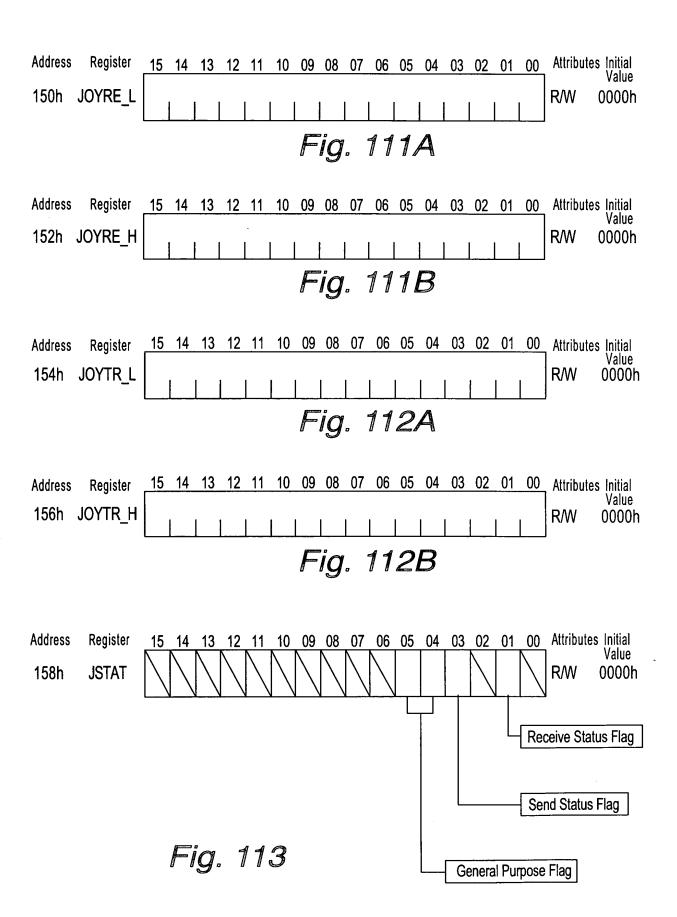


Fig. 110



Device Reset

Direction	Order	d7	d6	d5	d4	d3	d2	d1	d0	Remarks
Receive	1	1	1	1	1	1	1	1	1	Command 255(FFh)
i	1	0	0	0	0	0	0	0	0	Type Number
Send	2	0	0	0	0	0	1	0	0	0400h
	3			Lower 8	B bits of	Registe	r JSTAT			Communication Status

Fig. 114

Type/Status Data Request

Direction	Order	d7	d6	d5	d4	d3	d2	d1	d0	Remarks
Receive	1	0	0	0	0	0	0	0	0	Command 0(00h)
	1	0	0	0	0	0	0	0	0	Type Number
Send	2	0	0	0	0	0	1	0	0	0400h
<u>.</u>	3			Lower 8	bits of	Registe	r JSTAT			Communication Status

Fig. 115

AGB Data Write

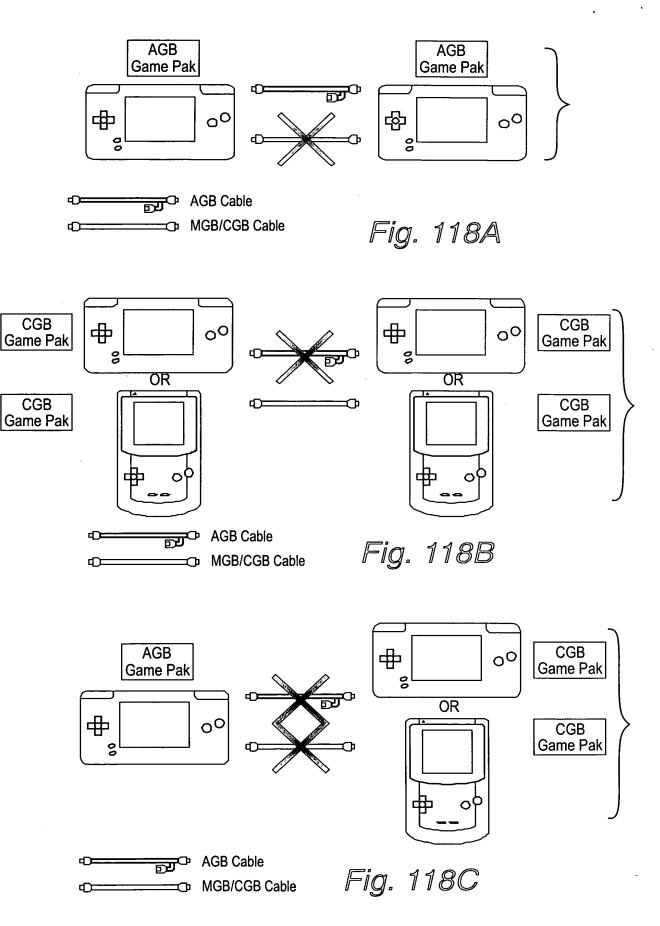
Direction	Order	d7	d6	d5	d4	d3	d2	d1	d0	Remarks
Receive	1	0	0	0	1	0	1	0	1	Command 21(15h)
	2		Lower	3 bits of	receive	data Re	gister JC	OYRE_L		
Receive	3		Upper	8 bits of	receive	data Re	gister JC	YRE_L		Receive Data
Receive	4		Lower	B bits of	receive	data Re	gister JC	DYRE_H		Neceive Dala
	5		Upper	8 bits of	receive	data Re	gister JC	YRE_H		
Send	6			Lower 8	3 bits of	Registe	JSTAT			Communication Status

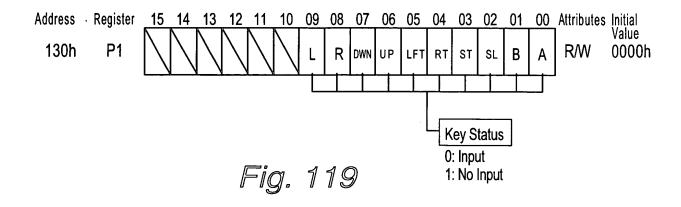
Fig. 116

AGB Data Read

Direction	Order	d7	d6	d5	d4	d3	d2	d1	d0	Remarks
Receive	1	0	0	0	1	0	1	0	0	Command 20(14h)
	2		Lowe	8 bits o	f send c	lata Reg	ister JO	/TR_L		
	3		Uppe	r 8 bits c	f send d	ata Reg	ister JO\	/TR_L		Send Data
Send	4		Lower	8 bits o	f send d	ata Regi	ster JO	YTR_H		Seria Dala
	5		Uppe	r 8 bits o	f send d	ata Regi	ster JOY	TR_H		
	6			Lower	3 bits of	Registe	r JSTAT	<u> </u>		Communication Status

Fig. 117





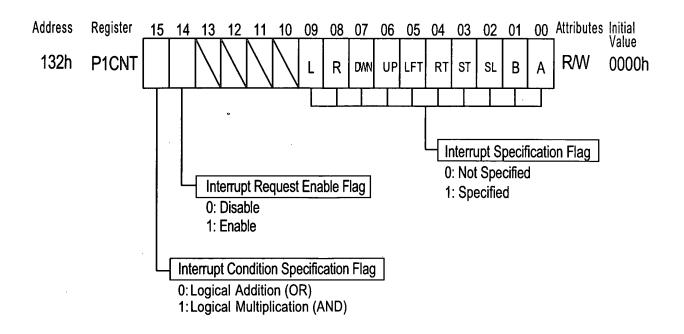
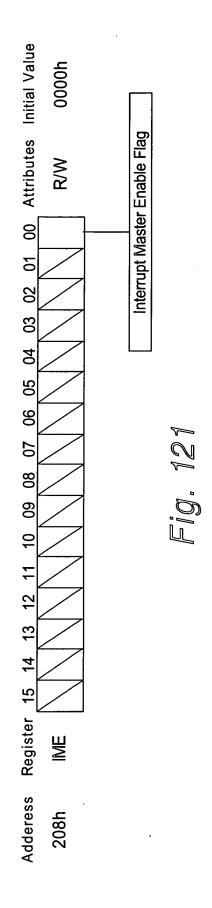


Fig. 120



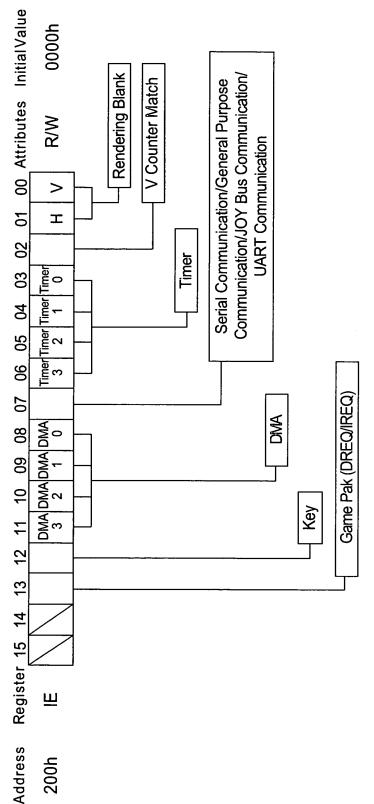


Fig. 122

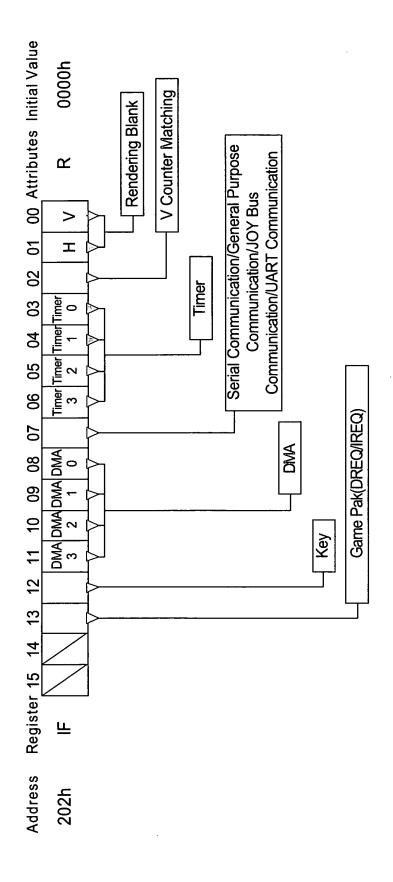


Fig. 123

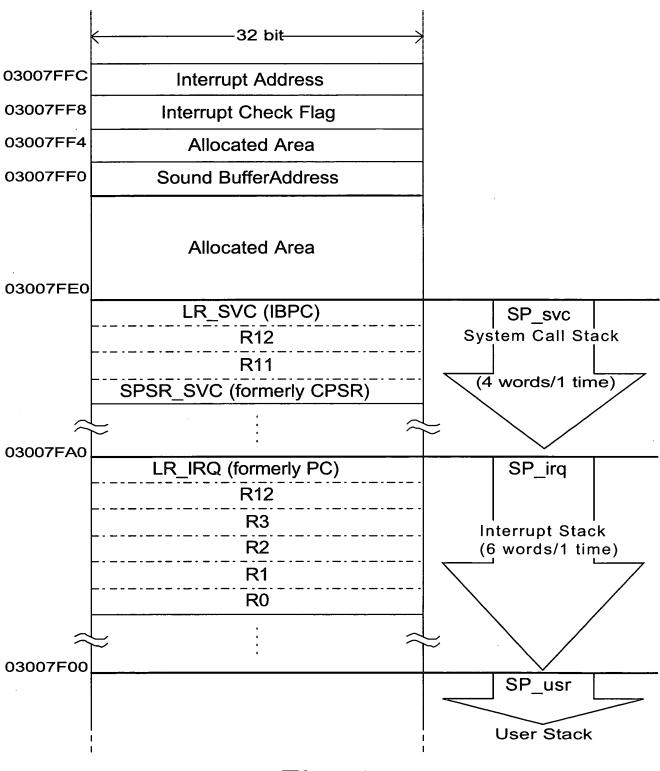
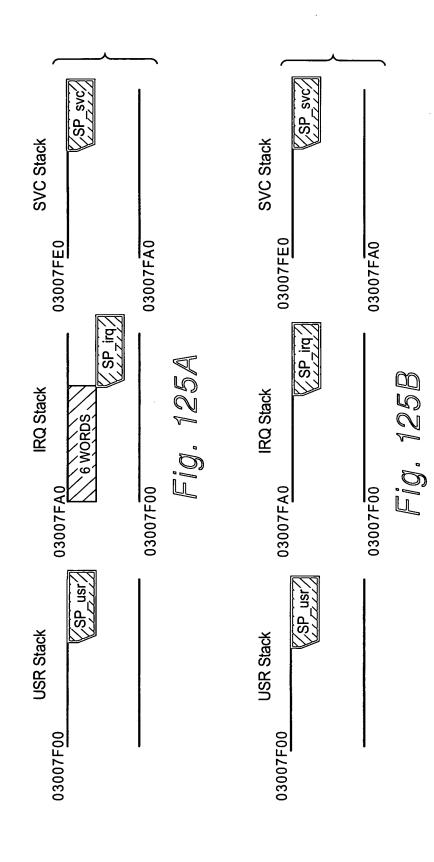
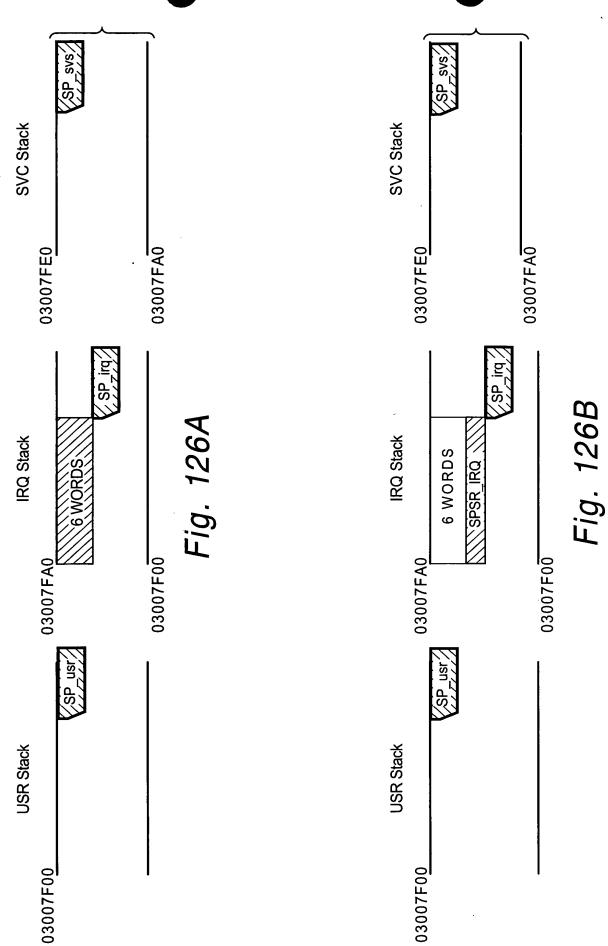
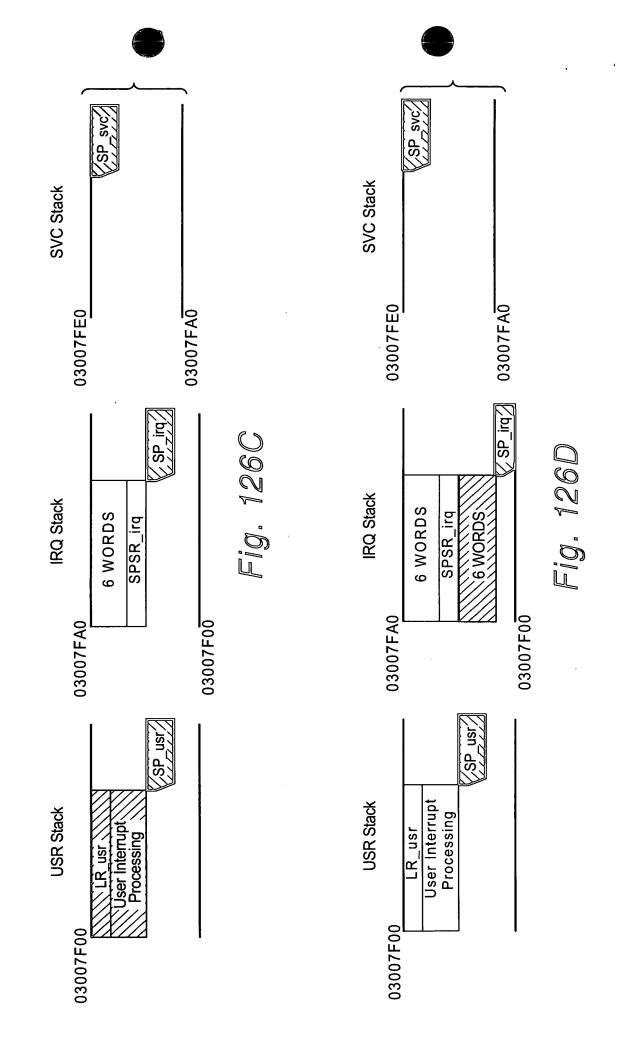


Fig. 124







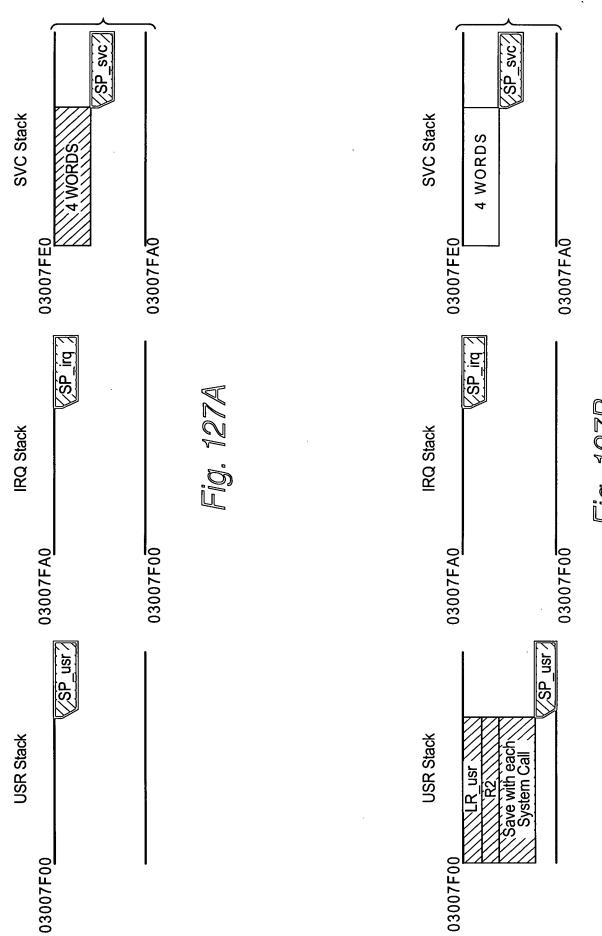


Fig. 127B

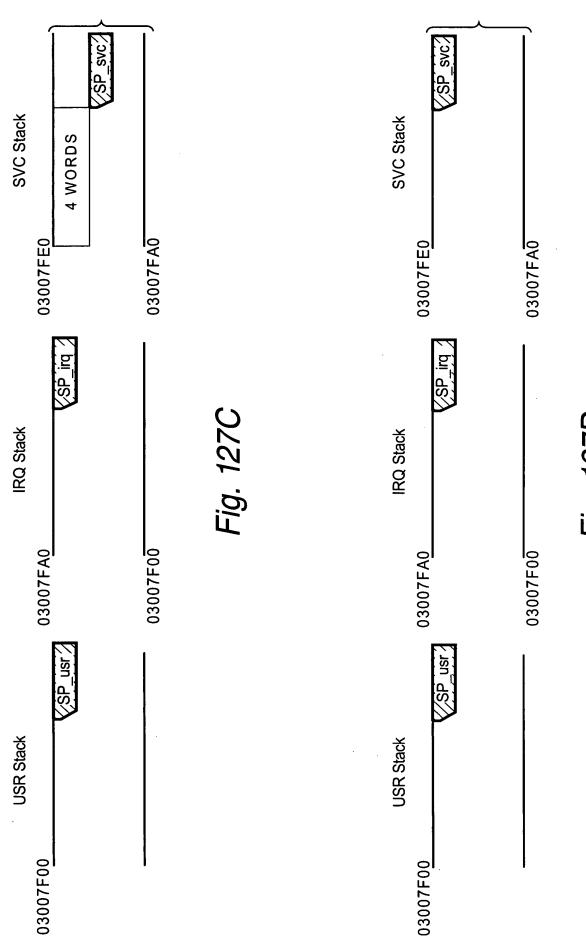


Fig. 127D

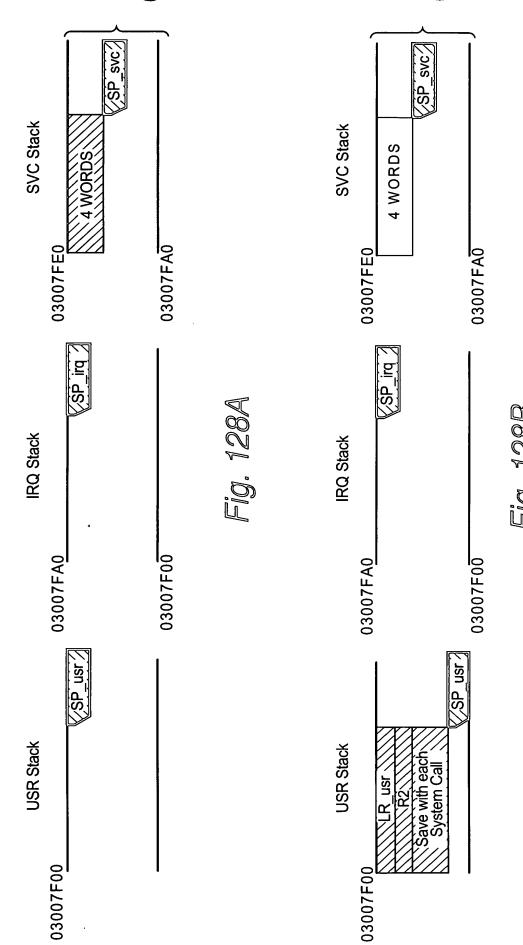
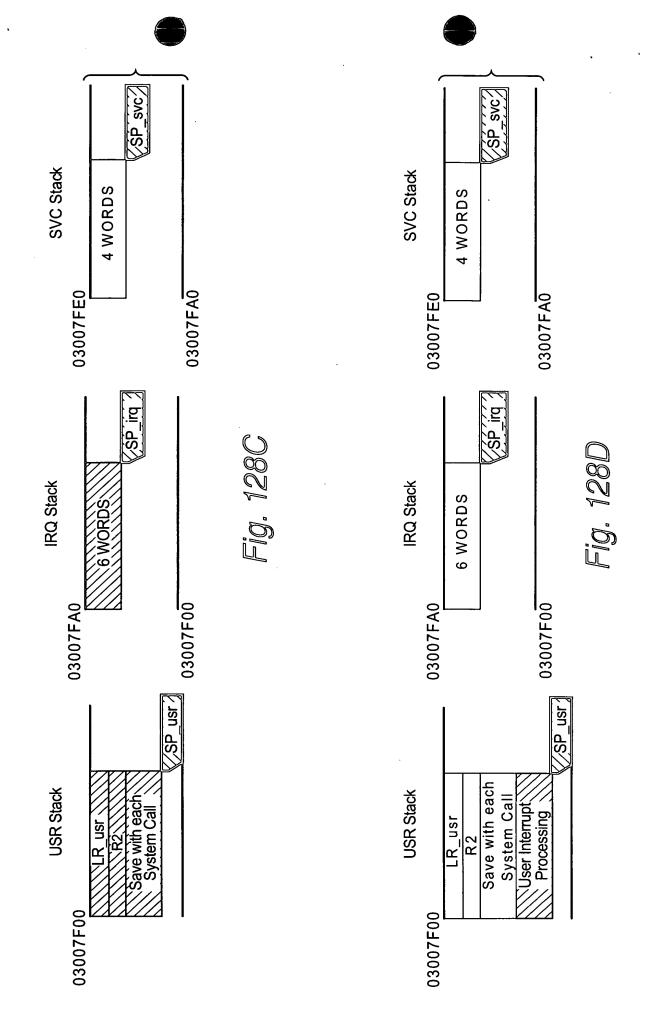


Fig. 128B



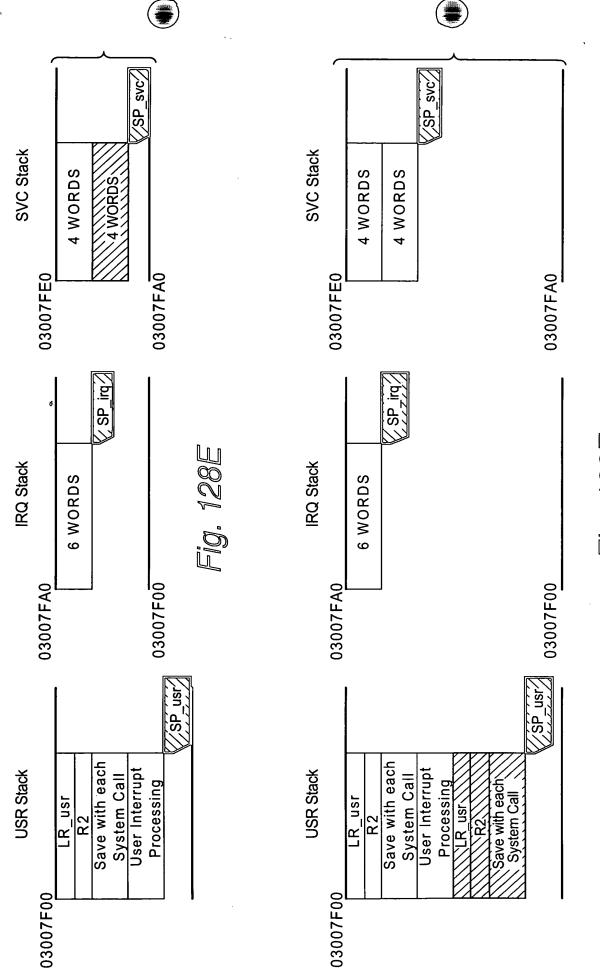
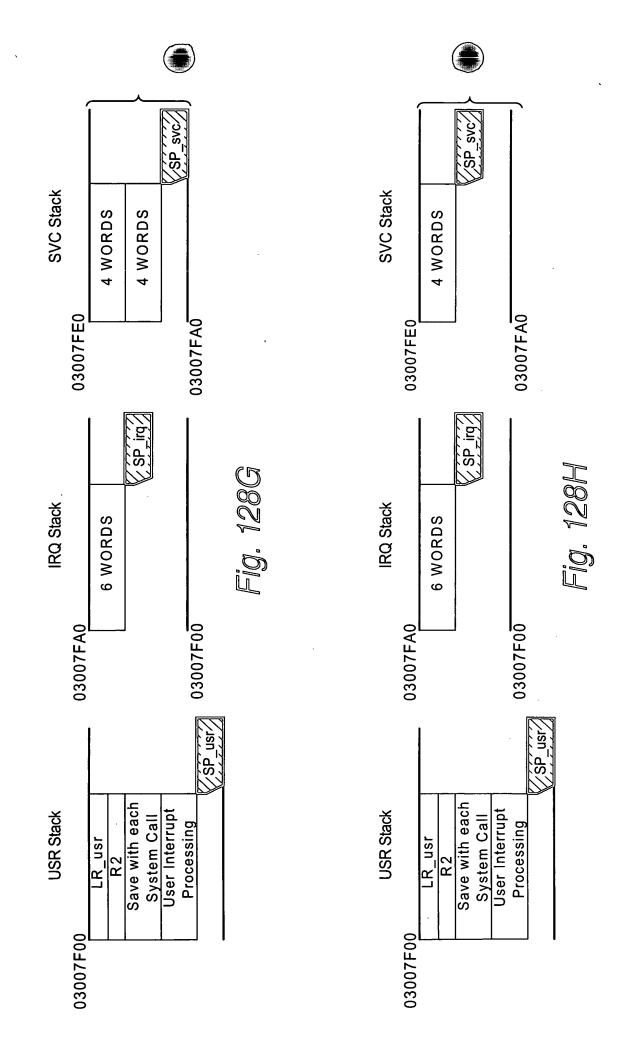
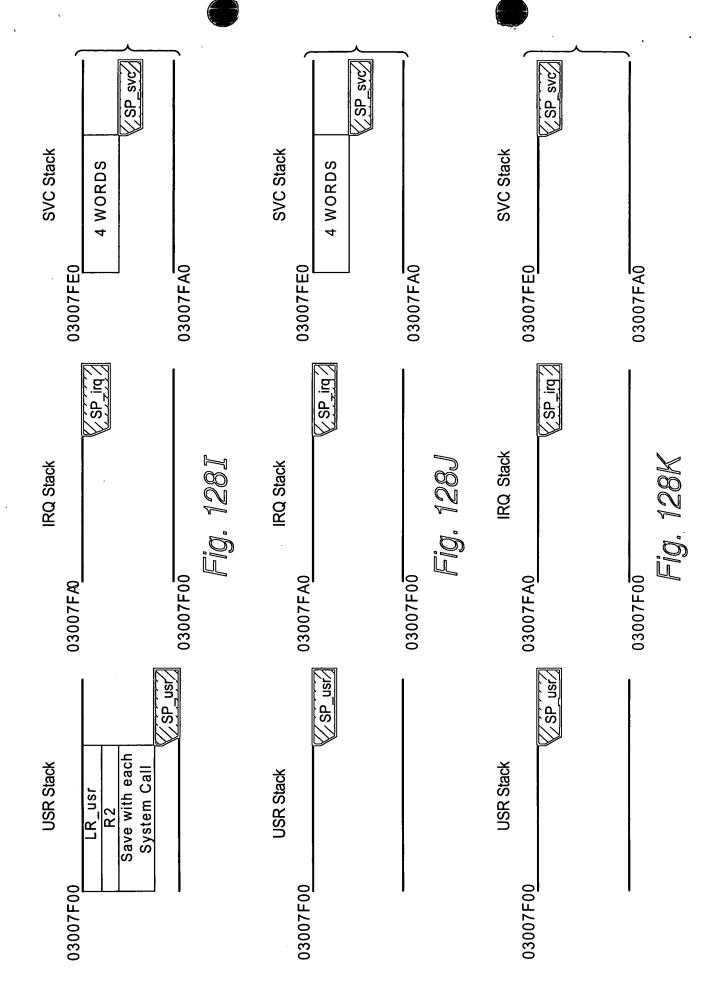


Fig. 128F





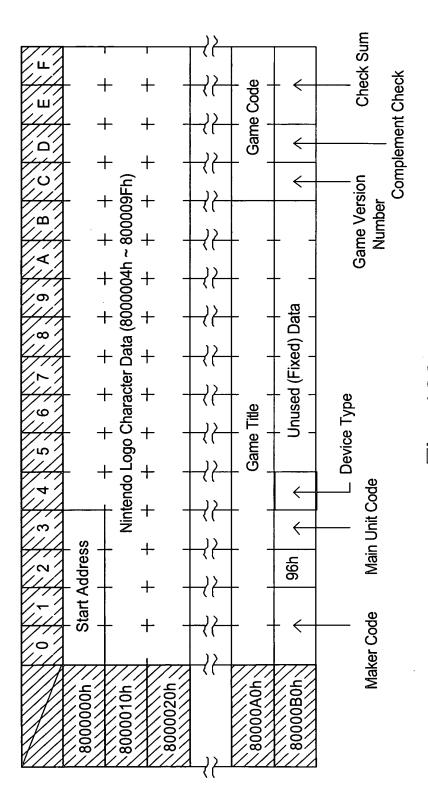
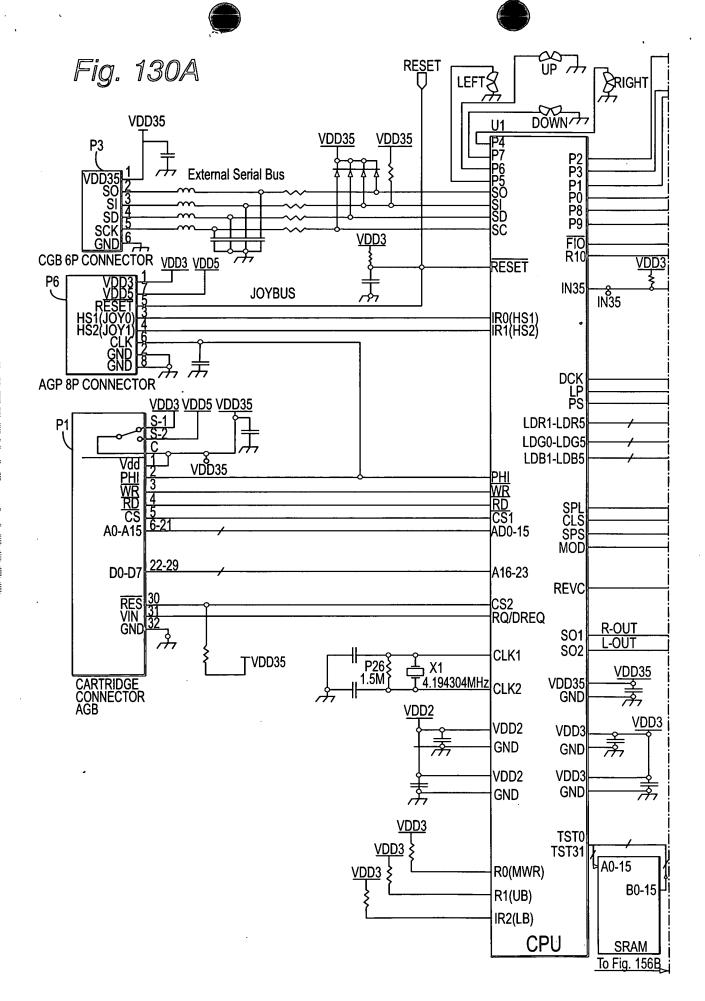
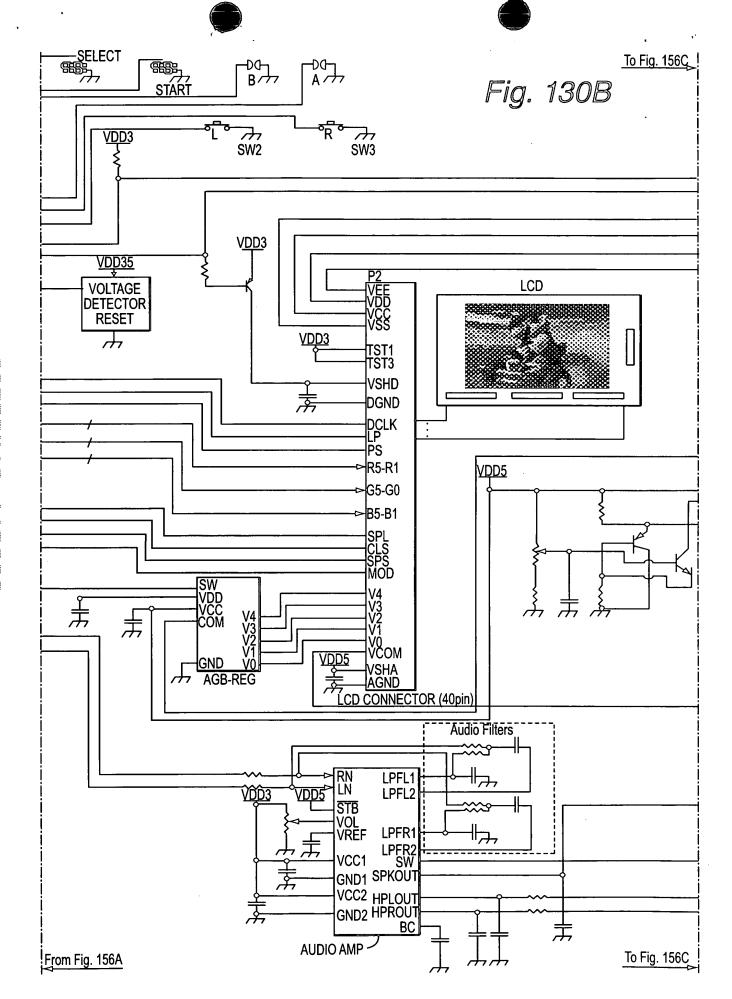


Fig. 129





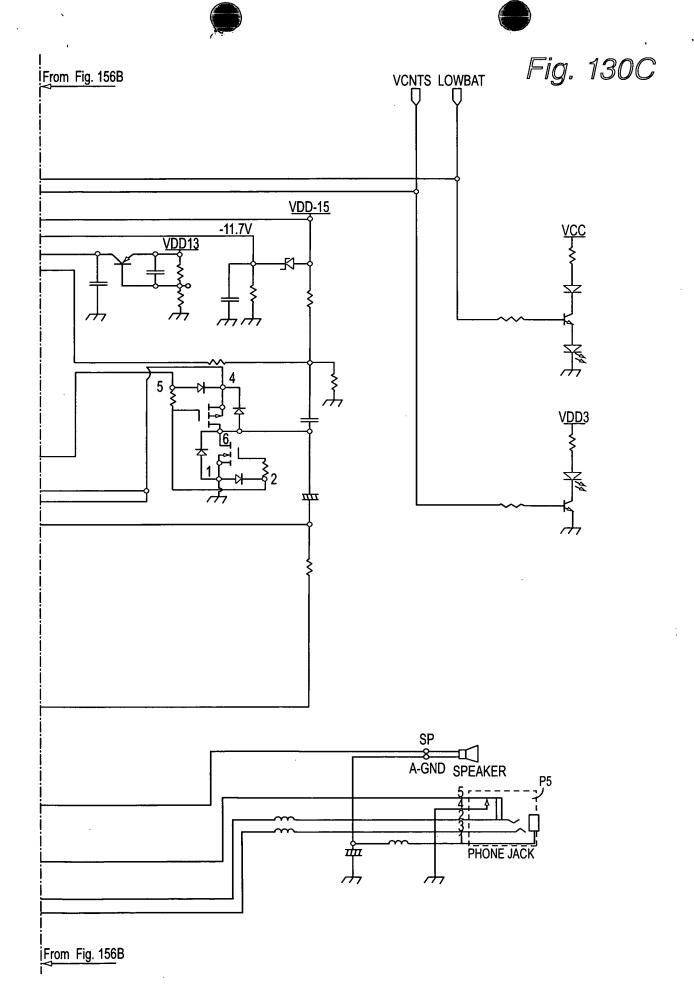


Figure in App,	ë	X	i≅i‰	2,E	₩Ę ŻĠ	Şğ. Şğ.	E-85	32B 32B	Fig. 45A	55. 39. 19.	Ē.₹	5.65 B.	₽. 55. 6.	45B 45B	₽. 5. 5. 5.	5.65 E-66	₽ <u>₩</u>	5.4 8.0	15.4 15.5	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Initial- Value ii	USO.		10000	40000	40000	40000	40000	40000	0000h	10000	40000	40000	40000	10000	40000	40000	0100h	10000	0100h	10000
R/W	MA	1441	R/W	Y.	RW	RW	RW	RW	M	M	8	Μ	Μ	M	M	8	3	3	3	8
000			VBlank Status	,																
100	RG Mhda	O WOOG	HBlank Status		Priority	Priority	Priority	Priority												
D02		.	Counter Eval		.Base	.Base	Base *	.Base k												
D03	egy)	apau	VBlank Interrupt	.Value	Character Base Block	Character Base Block	Character Base Block	Character Base Block	¥		+ =:		±.		755					
D04	Frame	No .	HBlank Interrupt	V Counter Value	0	0	0	0.	Horizontal Offset	Vertical Offset	Horizontal Offset	Vertical Offset	Horizontal Offset	Vertical Offset	Horizontal Offset	Vertical Offset				
D05	ິງ ສີ	Hoff	V counter Match Interrupt		0	0	0	0	Horiz	Verti	Horiz	Verti	Horiz	Verti	Horiz	Verti	ction	ection	ction	ection
900	OBU Man	Format			Mosaic	Mosaic	Mosaic	Mosaic									dx: Distance moved Along same line in x direction	dmx: Distance moved Along next line in x direction	dy. Distance moved Along same line in y direction	dmy: Distance moved Along next line in y direction
D07	Forced	Blank	,		Node Mode	Color Mode	Wode Wode	Color Mode									same lin	ng next lir	same lin	ng next lir
D08		BG0		•			-										ved Along	oved Alor	ved Along	oved Alor
600		BG1		•	Block	Block	Block	Block	•	•	•	•	•	•	•		nce mo	tance m	nce mo	tance m
D10	Display Flag	BG2		-	Base	Base	Base	Base	•	•	•	•	•	•	•		dx: Dista	dmx: Dis	dy: Dista	dmy: Dis
D11	Ö	BG3	etting	•	Screen	Screen	Screen	Screen	•	•	,	•	-	-	-					
D12		0BJ	V Count S	•					•		•	•	•	•	•					
D13	Flag	WIND	٨		•	•	Area Overflow	Area Overflow	•	• . '		•	,	•	-	•				
D14	Window Display Flag	W IN1					a			•				•	•	•				
D15	Window	08)		•	Size	Size	Size	Size	•	,	,	•	,		•	,				
	DISPCNT	200	DSPSTAT	VCOUNT	BGOCNT	BG1CNT	BG2CNT	BG3CNT	BGOHOFS	BGOVOFS	BG1HOFS	BG1V0FS	BG2H0FS	BG2V0FS	BG3H0FS	BG3VOFS	BG2PA	BG2P8	BG2PC	BG2PD
Addr	W	3	70	90	80	₩	႘	30	10	12	14	16	18	14	10	Ħ	20	22	74	26



in App	Ē.&	Fig. 438	Fig.	당 당	ē. <u>₹</u>	무원	₽. <u>4</u>	등 <u>4</u>	<u>6</u> . \$	당 연	Fig. 30.	£9. 39.	_			_	95. 65.	. <u>E</u> ,68
Initial- Fig. Value in App	10000	0000h	0000h	10000	0100h	40000	0000h	0100h	40000	0000	40000	0000h	10000	0000h	40000	40000	R/W 0000h	R/W 0000h
RW		W		W	W	W		M		W		W	M	W	M	W	RW	RW
000																!	BG 0	BG 0
- BO									-								BG1	BG 1
D02											:		ate	ate	ate	ate	BG2	BG 2
D03		ults)		sults)						lts)	i	saults)	Window 0 lower-right x-Coordinate	Window 1 lower-right x-Coordinate	Window 0 lower-right y-Coordinate	Window 1 lower-right y-Coordinate	BG3	BG 3
P94	(s)	x-Coordinate of referenceStarting point (rotation/scaling results)	llts)	y-Coordinate of reference Starting point (rotation/scaling results)					(6	Starting point (rotation/scaling results)		Starting point (rotation/scaling results)	wer-right >	wer-right)	wer-right)	wer-right)	OBJ	0B J
D05	ling result	rotation/s	aling resu	(rotation/					ng results	(rotation/s	esults)	: (rotation	ol 0 wobi	ol 1 wobu	ol 0 wobi	ol 1 wob	Special Effects	Special Effects
900	tation/sca	ing point (otation/sc	ting point	rection	irection	rection	irection	ation/scali	rting point	/scaling r	rting point	Wir	Wir	Wir	Wir	•	•
D07	x-Coordinate of referenc&tarting point (rotation/scaling results)	enceStarti	Starting point (rotation/scaling results)	ence Star	dx: Distance moved Along same line in x direction	dmx: Distance moved Along next line in x direction	dy: Distance moved Along same line in y direction	dmy: Distance moved Along next line in y direction	Starting point (rotation/scaling results)		Starting point (rotation/scaling results)						•	•
80G	ıc&tartinç	te of refer	Startin	te of refer	ing same	long next	ing same	long next	Starting	x-Coordinate of reference	arting poin	y-Coordinate of reference					BG0	BG0
600	of referer	-Coordina	ence	-Coordina	noved Alc	moved A	noved Alc	moved A	auce	x-Coordina		y-Coordina					ow1 BG1	BG1
D10	oordinate	X	rdinate of reference	У	Distance	: Distance	Distance	: Distance	x-Coordinate of reference		y-Coordinate of reference		dinate	dinate	dinate	dinate	Inside of Window 1 G3 BG2 E	Window Control 3G3 BG2
D11)-x		y-Coordina		жр	dmx	dy:	dmy	(-Coordina		/-Coordina		Window 0 upper-left x-Coordinate	Window 1 upper-left x-Coordinate	Window 0 upper-left y-Coordinate	Window 1 upper-left y-Coordinate		OBJ Wind
D12		•	y.	•						•	1	•) upper-le	l upper-le) upper-le	l upper-le	Control for OBJ B) OBJ
D13		•		•						•		٠	Window (Window 1	Window (Window 1	Special Effects	Special Effects
D14				•						•		•					•	•
015		•		•						•		•		-			•	•
Register	BG2X _L	BG2X_H	BG2Y_L	BG2Y_H	BG3PA	ВСЗРВ	ВСЗРС	везрр	BG3X_L	BG3X_H	BG3Y_L	ВСЗУ_Н	WINOH	WIN1 H	WINOV	WIN1 V	WININ	WNOUT
Addr	28	2 2A	30	Œ	99	32	ਲ	99	88	3A	30	3E	40	42	4	46	48	4A

Fig. 28

Fig.	Ēģ₩	Fig.	<u>5</u> ,88	E.68	₽'n	₽ <u>.</u> 62	₽.K	₽₽₽	흔		먇뚄	팔	Ē.Ķ	:EK	₽₽	: <u>5,</u> %	E.K	:E,&;
Initial-I Fig. Value in App	0000h	40000	10000	40000	10000	40000	W/R 0000h	W/R 0000h	1000 1000	W/R 0000h	W/R 0000h	W/R 0000h	1000 1000	W/R 0000h		W/R 0000h	900	0000h
RW	W	RW		*	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R	WIR	W/R	W/R	W/R
000		1 BG 0	EVA	EW												Sound 14 Mix Ratio		
D01	I Size	BG 1	efficient	efficient										:				
D02	Horizontal Size	1 st target pixel BG3 BG2	Color Special Effect Coefficient EVA	Color Special Effect Coefficient EVY												DSA Output Ratio		
D03	osaic 	1 st tarç BG 3	Specia	Specia	0	=	က	_	8	0 ~		33	-	°	0.9	Ratio DSB Articipated	2 5	
D04	BG Mosaic	OB]	S	Sol	NR1 0	NR11	NR1 3	NR2 1	NR2 3	NR3 0	NR3 1	NR3 3	NR4	NR4 3	NR5 0		NR5 2	le
D05	l Size	80	•															Bias Level
D06	Vertical Size	Type of Color Special Effect	•													•		
D07		Type Specii	•	•														
800		BG 0			•					•						Output		
600	I Size	BG 1	Color Special Effect Coefficient EVB	•	•											nd A Output		
D10	Horizontal Size	et pixel BG 2	fect Coef	•			1						:			Direct Sound A	1	•
011		2nd target pixel BG3 BG2	Special Ef	•		5	4	2	4		~	4	2	4	_	Direct Sound FIFO A TIMER reset	•	•
D12	OBJ Mosaic 	0B J	Color	•		NR12	NR14	NR22	NR24		NR32	NR34	NR42	NR44	NR51		ŀ	•
D13	Vertical Size	80	٠		•											and B Output		•
014	Vertic	•	•													Direct Sound B		Resolution/ g Cycle
015		•	•	•	•					•						FIFO B	•	Amplitude Resolution/ Sampling Cycle
Register	MOSAIC	ВГРМОР	COLEV	COLEY	SG10_L	SG10_H	SG11	SG20	SG21	7_0698	N_0502	SG31	SG40	SG41	SGCNT0_L	SGCNT0_H	SGCNT1	SGBIAS
Addr	40	20	25	끃	8	62	22	88	႘ွ	22	72	74	82	22	8	82	\$	88

Fig.

Addr	Register	D15	D14	D13	D12	D11	D10	600	800	D07	900	D05	D04	D03	D02	D01	000	R/W Initial-		Fig.
8	SGWR0_L		Step 2	2			Step 3	p 3			Ste	Step 0			ੈੱਡ 	Step 1		W/R		Fig. 76A
95	SGWR0_H		Step 6	9			Step 7	p 7			Ste	Step 4			**************************************	Step 5		W/R	•	Fig. 76B
82	SGWR1_L		Step 10	10			Ste	Step 11			វ័ ភ	Step 8			វ័ ភ	Step 9		WR	•	Fig. 760
8	SGWR1_H		Step 14	14			Ste	Step 15			Ste 	Step 12			ੈੱਡ 	Step 13		W/R	1	Fig. 76D
88	SGWR2_L		Step 18	18			Ste	Step 19			Ste	Step 16			*	Step 17		WR		Fig.76E
8	SGWR2_H		Step 22	22			Ste	Step 23			Ste	Step 20			žš	Step 21		W/R	•	Fig. 76F
င္တ	SGWR3_L		Step 26	26			Ste	Step 27			Ste	Step 24			ξξ	Step 25		X/R	•	Fig.76G
띯	SGWR3_H		Step 30	30			Ste	Step 31			Ste	Step 28			\ \	Step 29		W/R	1	Fig. 76H
8	SGFIFOA_L			Š	Sound Data	ıta 1						Sot	Sound Data0	e e				>	,	Fig. 71A
¥ 2	SGFIFOA_H			တ	Sound Data 3	ıta 3						So	Sound Data2	72				3	-	Fig. 72A
₩	SGFIFOB_L			S	Sound Data	ita 1						Sol	Sound Data 0	0.1				3	'	Fig. 71A
9e	SGFIFOB_H			Ń	Sound Data 3	ıta 3						Sol	Sound Data 2	12				3	•	Fig. 72A
B0	DM0SAD_L															:) M	0000h Fig. 82A	ig. 82A
B2	DM0SAD_H	•	•	•	•	•												3	0000h Fig. 82B	ig. 82B
B4	DM0DAD_L																	3	0000h Fig. 83A	ig. 83A
98 8	DM0DAD_H	•	•	•	•	•												8	0000h Fig. 83B	ig. 83B
88 88	DM0CNT_L	•	•															M		Fig.84
BA	DM0CNT_H Enable Interrupt Startup Timing	Enable	Interrup	nt Startu	p Timing	•	Transfe Width	Contin	DMA 0 Control Source Add Luous Contro	Control urce Add Control	DMA 0 Control Transfer Continuous Source Address Destination Width Address Control Address Addres	ess Cont	- - - -	,	·	•	1	W/R	W/R 0000h	Fig.85

in App.	ig. 86A	ig. 86B	ig. 87A	ig. 87B	Fig. 88	Fig. 89	ig. 86A	ig. 86B	ig. 87A	ig. 87B	Fig. 88	Fig. 89	ig. 90A	ig. 90B	ig. 91A	ig. 91B	-ig. 92	-ig. 93
Initial- Value	0000h Fig. 86A	0000h Fig. 86B	0000h Fig. 87A	0000hFig. 87B		1 40000	0000hFig. 86A	0000h Fig. 86B	0000h Fig. 87A	0000h Fig. 87B		0000h Fig. 89	0000h Fig. 90A	0000h Fig. 90B	0000h Fig. 91A	0000h Fig. 91B	0000h Fig. 9	W/R 0000h Fig. 93
RW	W	W	M	M	W	W/R	W	W	W	W	W	W/R	W	M	M	M	M	W/R
000						•						•						
D01						•						•						
D02						•						•						•
D03						•						•						•
D04		:				•						•						•
D05						ation Control						nation Control						lation Control
900						Destination Address Control						2 Control Contin- Source Address Destination uous Control						Destination Address Control
D07	ddress	ddress	DMA 1 Destination Address	DMA 1 Destination Address	ıţ.	1 Control Contin- Source Address uous	ddress	ddress	DMA 2 Destination Address	DIMA 2 Destination Address	Jt	Address	ddress	ddress	DMA 3 Destination Address	DMA 3 Destination Address	π	3 Control Contin- Source Address uous Control
D08	DMA 1 Source Address	DMA 1 Source Address	estinatior	estinatior	Word Count	ol - Source Co	DMA 2 Source Address	DMA 2 Source Address	estinatior	estinatior	Word Count	ol - Source Co	DMA 3 Source Address	DMA 3 Source Address	estinatior	estinatior	Word Count	ol Source Co
60 0	DMA 1	DMA 1	DMA 1 D	DMA 1 D	Λ		DMA 2	DMA 2	DMA 2 D	DMA 2 D	^		DMA 3	DMA 3	DMA 3 D	DMA 3 D	٨	
D10						DMA Transfer Width						DMA Transfer Width						DMA Vansfer Width
D11				•		•				•		•						DREQ
D12		•		•		p timing		•		•		p timing		•		•		timing
D13		•		•		Startu		•		•		Startu		•		•		Startup
D14		•		•		Interrupt		•		•	•	Enable Interrupt Startup timing						Enable Interrupt Startup timing DREQ
D15		,		•	•	Enable		•		•	•			•		•		Enable
Register	DM1SAD_L	DM1SAD_H	J_OAO1MO	DM1DAD_H	DM1CNT_L	DM1CNT_H Enable Interrupt Startup timing	DM2SAD_L	DM2SAD_H	DM2DAD_L	DM2DAD_H	DM2CNT_L	DM2CNT_H	DM3SAD_L	DM3SAD_H	DM3DAD_L	DM3DAD_H	DM3CNT_L	D3CNT_H
Addr	BC	1 13 15	ප	73	2	9	జ	CA	သ	3	20	02	D4	90	80	DA	20	DE

Ago.in	g. 81/	ig. 81E	g. 81/	ig. 81E	ig. 81/	ig. 81E	g. 81/	g. 81E
<u>e</u> <u>a</u>	0000h Fig. 81A	0000h Fig. 81B	0000h Fig. 81A	0000h Fig. 81B	0000h Fig. 81A	0000h Fig. 81B	0000h Fig. 81A	R/W 0000h Fig. 81B
V Ini	 	8		00 /)0 >		00
8	≥	RW	>	R/W	W	R/W	W	<u>8</u>
D12 D11 D10 D09 D08 D07 D06 D05 D04 D03 D02 D01 D00 R/W Ualua Value		Prescalar		Prescalar		Prescalar		Prescalar
2								
D02		Count Up Timing		Count Up Timing		Count Up Timing		Count Up Timing
D03				_				
D04								•
D05		-		-				-
D06		Interrup		Interrup		Interrup		Interrup
D07	Timer 0 Setting	r 0 Control Operation Interrupt	Timer 1 Setting	imer 1 Control - Operation Interrupt	Timer 2 Setting	Timer 2 Control Operation Interrupt	Timer 3 Setting	r 3 Control Operation Interrupt
D08	Timer 0	Timer 0 Control	Timer 1	Timer 1 Control	Timer 2	Timer 2 - O _l	Timer 3	Timer 3 Control
D09				•		ı		•
D10		•		•	٠			•
D11				•				•
D12		•		•				•
D13				• 		•		
								•
015				•		•		•
Addr Register D15 D14	TMOD	TM0CNT	TM1D	TM1CNT	TM2D	TM2CNT	TM3D	TM3CNT
Addr	\$	102	\$	106	108	10A	100	10E

Fig. 131F

	,														
Fig. in Abb.	Fig. 97A	Fig. 97B	Fig. 104C	Fig. 104D		85 E			!	rig. 90	Fig. 119		Fig. 120	Fig. 100	
Initial- Value	0000h	0000h	0000h	10000		0000h	0000h	0000h		0000h	0000		0000h	HUUUU	2000
RW	RW	RW	RW	RW		RW	R/W	RW.		RW	RW		RW	AVO	<u>*</u>
D0 0						Social Participation	Baud Rate	Baud Rate			¥		А		SC
D01						NOSE PESSE P	Band	BB &B			В		В	둞	S
D02						Transfer Frable Receive	Si Terminal Monitor	CTS Flag)ata	Select		Select	Data Bit	<u></u>
D03	ata 0	ata 1				Transfer Frable Send	SD Terminal Monitor	Parity Control		8Bit Normal SIO Communication Data	Start		Start		SS
D04	ication Da	ication Da				•		Send Data Flag		O Comm	~		æ		သွ
500	Commun	Commun	2	₆₀	ltrol	•	Multi-play ID	Receive Data Flag		Normal SI		•		Input/Output Select	S
900	Multi-play	Multi-play	tion Data	tion Data	SIO Control	•	Comm- unication Fror Flag	Error Flag	n Data	8Bit	ತ್ತಿ		하	Input/Out	S
D07	Data and	Data and	mmunica	mmunica		Start	Start (master) Busy (slave)	Data Length	Communication Data		Down		Down		SO
D08	unication	unication	Multi-play Communication Data 2	Multi-play Communication Data 3		•	•	Elase Flage	දි	•	<u>~</u>	Key Interrupt	~	Interrupt	Enable
D09	Normal SIO Communication Data and Multi-play Communication Data 0	Normal SIO Communication Data and Multi-play Communication Data 1	W	W		•	•	Parity Flag		•	_	Key			
D10	Vormal SI	Vormal SI				•	•	Send Frable Flag		•	•	-	9		1
011	32-Bit	32-Bit				•	•	Receive Enable Flag		•	•		•		
D12		:				Transfer Bit Length	0	-		•		i	•		1
D13 D12						0	_	-		•	•		•	•	1
D14					Port Control	Interrupt Enable	Interrupt Enable	Interrupt Enable		•			Interrupt Enable	unication	Function Select
015						•	•	•		•	•	3	Condi-	Comm	Functi
Register	SCD0	SCD1	SCD2	SCD3	SCCNT_L	Normal SIO Communication	Multi-play Communication	UART Communication	SCCNT_H	Normal SIO Communication	₹.		P1CNT	Ω	=
Addr	120	122	124	126	128				12A		130		132	12	5

Fig. 131G

						T					r -		· ·		
Fig. in App.		Fig. 110	Fig. 111A	Fig. 111B	Fig. 112A	Fig. 112B		Fig. 113		Fig. 122		Fig. 123	Fig. 17	Fig. 121	
Initial- Value		0000h	0000h	0000h	40000	40000		40000		0000h		0000h	0000h	40000	40000
RW		RW	RW	RW	RW	RM M		RW.		RW.		RW	RW	RW	
000	Device	reset signal receive						•	:	V Blank		V Blank	SRAM Wait Control	Interrupt Master Flag	•
100		Receive Complete						Receive Status Flag	:	Blank		H Blank	SRAI	•	•
D02		Send Complete							:	Counter Match		Counter Match	00	•	•
D03	_							Send Status Flag		TMR0		TMR0	Wait State 0 Wait Control	•	•
D04	_	•						General Purpose Status Flag Flag		TIMR1		TMR1		•	•
500	_		0 8	a 1		_	sn	General	Flag	TMR2	Flag	TMR2			•
900	Control	Interrupt	eive Data	eive Data	and Data	and Data	eive Stat	•	t Enable	TMR3	Interrupt Request Flag	TMR3	Wait State 1 Wait Control		•
700	unication	ı	ation Rec	ation Rec	cation Se	cation Se	ation Rec		Interrup	Sio	Interrupi	Sio	WW	•	
800	JOY Bus Communication Control		JOY Bus Communication Receive Data 0	JOY Bus Communication Receive Data 1	JOY Bus Communication Send Data 0	JOY Bus Communication Send Data 1	JOY Bus Communication Receive Status			DWA 0		DWA 0		•	
600	JOY Bu	•)Y Bus C)Y Bus C	JOY Bus	JOY Bus	OX Bus C	•	Interrupt Enable Flag			DMA 1	Wait State 2 Wait Control	•	
D10	_	•))()	•		DMA 2		DMA 2	MM M	•	•
D11		1	,					1		DIMA 3		DMA 3	PHI Terminal Output Control	•	•
D12 .	_									Key		Key	E S S	•	•
D13	_						ļ	•		Game Pak		Game Pak		•	•
D14	_	•						•					Pre- fetch	•	Mode
D15		•						•		•		•	Game Pak Type	•	Power Down
Register		HS_CTRL	JOYRE_L	JOYRE_H	JOYTR_L	JOYTR_H		JSTAT		ш		뜨	WSCNT	IME	PAUSE
Addr		140	150	152	154	156		158		200		202	204	208	300

Fig. 131H

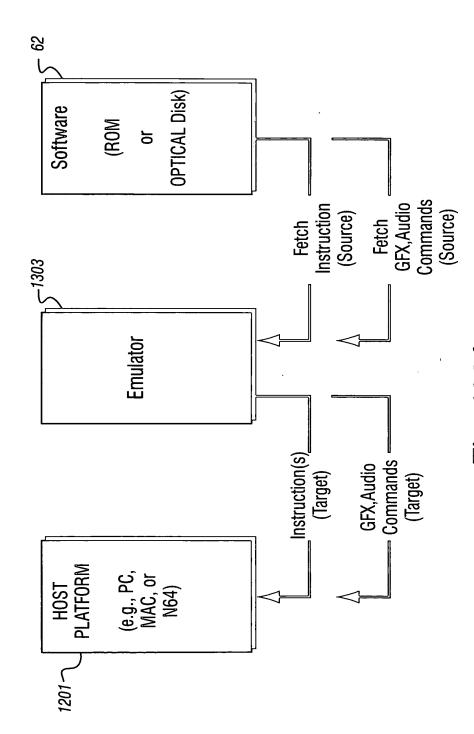
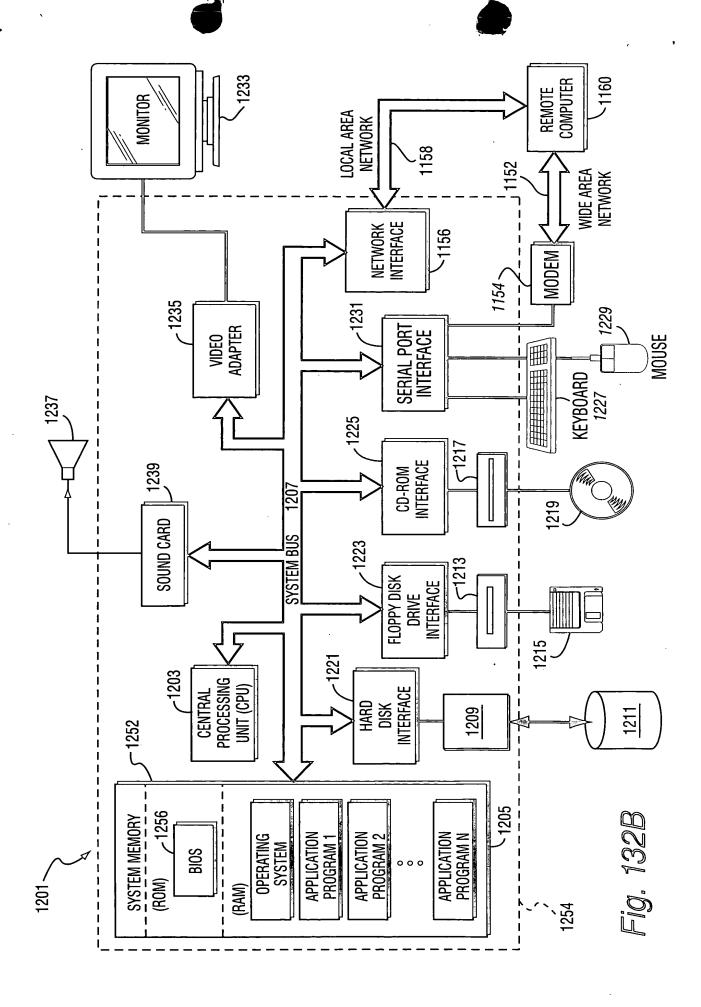
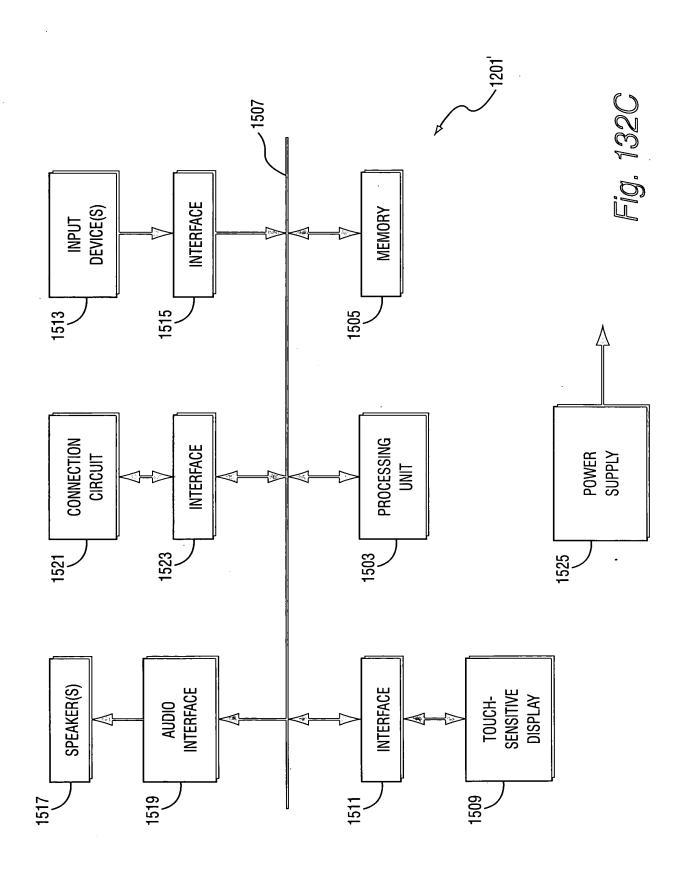


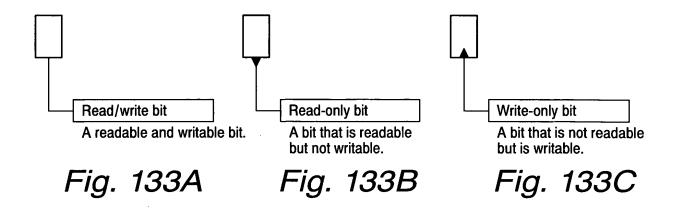
Fig. 132A











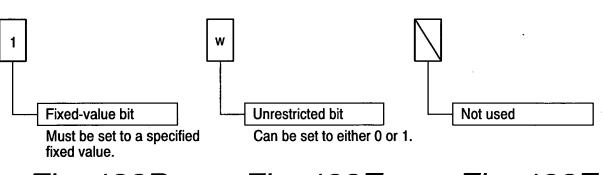


Fig. 133D

Fig. 133E

Fig. 133F